Implementation of Reusable
FM0/Manchester encoding using SOLS
 technique for DSRC Application

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Abstract

dedicated short range communication (DSRC) is an important technique which allows transmission of high data in communication based safety applications. To enhance signal reliability and to reach dc balance, DSRC standards uses either FM0 or Manchester coding technique. There is limitation on the hardware potential of existing DSRC system, because the code word structure for both FM0 and Manchester are different. SOLS technique is used to conquer this problem which combines the hardware architecture of FM0 and Manchester and this combined architecture gives Hardware utilization rate (HUR) to 100\%. We have implemented this design using 90nm CMOS technology in tanner tool. The power consumption of both FM0 and Manchester encoding is 15 \(\mu\text{W}\) and 1.86\(\mu\text{W}\) respectively. Delay for both 99nS and 0.2nS respectively. Keywords FM0, Manchester, Hardware utilization rate.

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1 INTRODUCTION

Dedicated short range communication is used to allow vehicles in intelligent transportation system to communicate with other vehicles and infrastructure to avoid the accidents. DSRC is used in vehicle to vehicle (V2V) and vehicle to infrastructure (V2I). In V2V, DSRC allows vehicles to communicate with each other. This communication is used for safety reasons such as to alert drivers of one car that is in front of another car. In V2I, there is communication between vehicles and infrastructure to enable security and can be used to collect toll and parking payments. DSRC baseband processor uses the FM0/Manchester coding for reliable communication and to maintain DC balance. The code word structure of both FM0 and Manchester encoding is different which limits the design of reusable architecture for both on a single hardware. Similarity Oriented Logic Simplification (SOLS) technique is used to conquer this problem. 100% HUR is achieved using SOLS technique.

As mentioned in [1] by P. Benabes, Manchester code generator running at a frequency of 1 GHz described. Using CMOS inverter and the gated inverter this design acts as switch to construct Manchester encoder and has the same complexity as standard D flip-flop. The Literature [3] replaces PMOS switch [1] with NMOS device. It is implemented using 90nm CMOS technology. In this design, switch size is smaller and reduces the parasitic capacitance due to removal of PMOS switch.

2 FM0 AND MANCHESTER CODING PRINCIPAL

Input data and clock for both FM0 and Manchester encoding denoted as X and CLK respectively, as shown in Fig 1. Using this parameter coding principle of FM0 and Manchester encoding described as follows.
Manchester encoding is also known as phase encoding. In Manchester encoding the transition from low to high represents logic 0 and transition from high to low represents logic 1 as shown in Fig 2. The Manchester encoder implemented using XOR operation between input data (X) and CLK.

Manchester Encoder = X ⊕ CLK.......(1)

For each input data FM0 code has two parts as former half cycle and later half cycle shown in Fig 1. Following three Rules exhibits for encoding of FM0 as:

Rule 1) If input data (X) is logic 0, then there must be a transition between A and B.
Rule 2) If input data (X) is logic 1, then there is no transition between A and B.
Rule 3) There must be a transition for each FM0 code no matter what input data is. Example of FM0 coding is given in Fig.3, which follows above three rules.

3 Hardware Architecture of FM0 and Manchester Encoder

Manchester encoder hardware architecture is simple as it is derived from XOR operation between input data and CLK. FM0 hardware architecture is not simple as that of Manchester encoder. So, by using FSM of FM0, the hardware architecture of FM0 can be designed. FSM of FM0 contains four states as S0, S1, S2 and S3. State code is given to each state as shown in Table I.

<table>
<thead>
<tr>
<th>State</th>
<th>Binary Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>11</td>
</tr>
<tr>
<td>S1</td>
<td>10</td>
</tr>
<tr>
<td>S2</td>
<td>01</td>
</tr>
<tr>
<td>S3</td>
<td>00</td>
</tr>
</tbody>
</table>

Based on coding principle of FM0, FSM of FM0 is as shown in Fig 4.

Fig.3. FM0 coding example
Consider state S1, its state code for A and B is 11. If input data (X) is at logic-0, state transition S0 and S2 follows the rule 1 and 3 and when input data (X) is at logic-1, then state S1 and S3 follows the rules 2 and 3. State transition for FM0 code is as shown in table II.

TABLE II. TRANSITION TABLE FOR FM0

<table>
<thead>
<tr>
<th>Previous State</th>
<th>Current State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A(t)</td>
</tr>
<tr>
<td>A(t-1)</td>
<td>X=0</td>
</tr>
<tr>
<td>B(t-1)</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

A(t) and B(t) denotes the current state at time ‘t’, where A(t-1) and B(t-1) denotes previous states. From table II A(t) and B(t) are given as:

A(t)=(B(t−1)).......... (2)
B(t)=X⊕(t−1) .............(3)

From (2) and (3) FM0 code can be given as,

FM0 Code=CLK A(t)+(CLK) B(t).............(4)

From (1) and (4) hardware architecture of FM0/Manchester encoder is shown in Fig.5. Top part of hardware architecture is FM0 encoder while bottom part shows the Manchester encoder.
Manchester encoding is simple and obtained by XOR operation between input data and CLK. But FM0 encoding is depends on X as well as previous state of FM0 code.

Hardware utilization rate can be calculated as,

\[ \text{HUR} = \left( \frac{\text{Active component}}{\text{Total component}} \right) \times 100 \] ...........(5)

4 REUSABLE VLSI ARCHITECTURE OF FM0 AND MANCHESTER ENCODING USING SOLS TECHNIQUE

By using two types of SOLS technique named as Area compact Retiming and Balance logic operation we get reusable hardware architecture of FM0 and Manchester encoding as shown in Fig.6.[9]

Fig.5. Hardware architecture of FM0/Manchester Encoding

Fig.6. Hardware architecture of FM0/Manchester encoding using SOLS Technique
5 HARDWARE UTILIZATION RATE WITH SOLS TECHNIQUE

The numbers of components are reduced when FM0/Manchester hardware architecture is designed using SOLS technique with two methods of SOLS design technique. All components are fully reused no matter which encoding technique is adopted. HUR of FM0/Manchester encoding with SOLS shown in table III.

<table>
<thead>
<tr>
<th>Coding</th>
<th>active component/total component</th>
<th>HUR</th>
</tr>
</thead>
<tbody>
<tr>
<td>FM0</td>
<td>5(44)/3(44)</td>
<td>100%</td>
</tr>
<tr>
<td>Manchester</td>
<td>5(44)/2(44)</td>
<td>100%</td>
</tr>
<tr>
<td>Average</td>
<td>5(44)/2(44)</td>
<td>100%</td>
</tr>
</tbody>
</table>

6 RESULT AND ANALYSIS

A. XNOR using 6T Transistor

We have implemented XNOR by using 6T transistors as shown in Fig.8. PMOS 8 and NMOS 8 are used to give or support strong 1 and strong 0 concepts.
B. D-FF Implementation in Tanner Tool

Hardware architecture of FM0/Manchester encoding using SOLS in Fig.6 designed using 22 transistors. We have designed D-FF using Conventional CMOS topology using only 17 transistors as shown in Fig.9. When CLR signal is 0, the output Q of DFF reset to 0 for Manchester encoding and when CLR signal is 1, then output of DFF is set to B(t-1) for FM0 encoding.

C. MUX using transmission Gate

2:1 Mux using transmission gate which requires only 6 transistors is implemented in Tanner tool. Depending upon MODE signal it selects either FM0 or Manchester encoding technique.

Fig.10 shows, the output waveform for the FM0/Manchester encoding. This design is implement using 90nm technology in Tanner Tool. We can observed that when Mode signal and CLR signal is 1 and 0 respectively then we get Manchester encoding technique and when Mode signal and CLR signal is 0 and 1 respectively then we get FM0 encoding technique.
7 COMPARISON WITH EXISTING DESIGN

The new modified DFF and XNOR design reduces transistor count from 44 to 37 as shown in table IV below. Which will further reduce the area and delay of this design, thus reducing power and transmission speed increases.

<table>
<thead>
<tr>
<th>Design Method</th>
<th>Coding</th>
<th>Active Component/Total Component</th>
<th>Average Transistor</th>
<th>HUR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Design</td>
<td>FM0</td>
<td>4(44)/4(44)</td>
<td>4(38)/7(98)</td>
<td>57.14%</td>
</tr>
<tr>
<td></td>
<td>Manchester</td>
<td>2(26)/1(98)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOLS Design</td>
<td>FM0</td>
<td>3(44)/3(44)</td>
<td>5(41)/5(44)</td>
<td>100%</td>
</tr>
<tr>
<td></td>
<td>Manchester</td>
<td>3(44)/3(44)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Modified SOLS Design</td>
<td>FM0</td>
<td>3(39)/3(39)</td>
<td>5(39)/5(39)</td>
<td>100%</td>
</tr>
<tr>
<td></td>
<td>Manchester</td>
<td>3(39)/3(39)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed SOLS Design</td>
<td>FM0</td>
<td>3(37)/3(37)</td>
<td>5(37)/5(37)</td>
<td>100%</td>
</tr>
<tr>
<td></td>
<td>Manchester</td>
<td>3(37)/3(37)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8 CONCLUSION

Hardware architecture of FM0 and Manchester encoding are different from each other, thus limitation on hardware utilization of reusable architecture design. SOLS technique overcome this limitation and improves HUR to 100%. The design is implemented in Tanner tool using 90nm technology. Modified XNOR and DFF design reduces overall transistor count from 44 to 37, which reduces area and delay of the proposed design. Power consumption for both FM0 and Manchester encoding is 15µW and 1.86µW respectively. Delay for FM0 encoding is 0.2nS and delay for Manchester encoding is 99nS. In future work we can implement this design in Quantum Cellular Automata (QCA), which provides a very high efficient computational platform than CMOS technology.
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