Simulation Analysis of New Symmetric Multilevel Inverter Topology with Reduced Number of Switches

V. Thiyagarajan
Department of EEE
SSN College of Engineering
Kalavakkam, Chennai, Tamilnadu.
thiyagarajanv@ssn.edu.in

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Abstract

The aim of this paper is to propose a new extendable symmetric inverter topology with minimum switch count. The basic unit of the proposed topology produces 5-level output voltage and it can be extended to synthesize greater output levels. The advantage of this topology is it uses minimum number of components and hence the cost and size of the inverter is reduced. In addition, the conduction loss is also minimum as compared with other presented topologies. The simulation results for different switching angle calculation methods are analysed and presented in this paper.

Key Words: Multilevel; Inverter; Symmetric; Switching angle; THD.

1 Introduction

Multilevel inverters synthesize a staircase waveform with the help of multiple dc sources and power switches [1]. The multilevel inverters are broadly classified into symmetric and asymmetric multilevel inverter [2]. In symmetric topology, the magnitude of all dc sources
are same whereas in asymmetric inverter, the voltage sources have different magnitude[3]. Multilevel inverters can be used in many applications such as photovoltaic systems, HVDC systems, FACTS and wind farms [4]. The various advantages of multilevel inverters are low distortion, low dv/dt stress, minimum switching losses, high power quality and minimum peak inverse voltage [5-7]. As the step number of the staircase waveform increases, the output waveform becomes smoother which closely resembles to the sinusoidal waveform. However, it requires larger number of power switches and gate drivers to synthesize higher number of output levels[8].

At first, the multilevel inverter was started with three level inverter topology and then several topologies of higher level inverter have been developed in recent years. The most popular topologies of multilevel inverters are diode-clamped[9], flying capacitor[10] and cascaded H-bridge inverters[11]. In modern days, many researchers has proposed many modified inverter topologies with improved performance for various applications [1-8, 12-14]. However, for higher output levels, these topologies increases the number of sources and power rating of the switching devices.

This paper proposes a new symmetric inverter topology. Section II explains the operating modes of the multilevel inverter topology. The different methods of calculating the switching angles are presented in Section -III. The simulation results are discussed in Section -IV. The conclusion is given in Section -V.

2 PROPOSED INVERTER TOPOLOGY

Fig. 1 shows the schematic diagram of the proposed inverter topology. It consists of two voltage sources and six switches. The proposed inverter can produce 5-level output voltage during symmetrical condition. Fig. 2 shows the different operating levels of the proposed inverter. During the positive level-1, the voltage V1 is obtained across the load. During this level, the switches S2 and S6 are ON and the other switches are OFF as shown in Fig.2 (a).
During the positive level-2 operation, the switches $S_2$ and $S_4$ are ON and the other switches are OFF to obtain the voltage is $V_1 + V_2$ as shown in Fig. 2(b). During the negative level-1, the voltage $-V_2$ is obtained across the load with the switches $S_3$ and $S_5$ are ON as shown in Fig. 2(c). During negative level-2, the switches $S_1$ and $S_3$ are ON. Therefore the voltage $-(V_1 + V_2)$ is obtained across the load as shown in Fig. 2(d). The zero voltage is obtained across the load either by turning ON the switches $S_1$ and $S_2$ or $S_3$ and $S_4$ as shown in Fig. 2(e) and Fig. 2(f) respectively. The generalised topology of the proposed inverter with 'n' dc sources and 'k' switches is shown in Fig. 3.
Fig. 2. Different levels of proposed inverter topology
The total output voltage obtained across the load terminals of the generalised inverter topology is given by,

\[ V_0 = \sum_{i=1}^{n} V_i \]  

(1)

The relationship between 'n' and 'k' is given by,

\[ k = n + 4 \]  

(2)

During symmetrical condition, the voltage magnitude of all sources is equal to Vdc. Therefore, the total number of levels 'm' obtained is given by,

\[ m = 2n + 1 \]  

(3)

From equation (2) and (3), the relation between 'm' and 'k' is given by

\[ m = 2k - 7 \]  

(4)
The plot between the number of levels vs switches and number of on-state switches vs number of sources are shown in Fig. 4 (a) and Fig. 4(b) respectively.

Fig. 4. Comparison (a) Levels vs Switches and (b) On-state switches vs Sources.

It is shown that the proposed inverter topology uses minimum number of switches to achieve greater output levels. It is also seen that only two switches are ON to synthesize any output level and it is lower than the conventional CHB inverter and other topologies presented in [2, 3, 5, 6, 13, 14]. This will reduces the number of associated gate driver circuits, installation area and overall cost of the proposed inverter topology. Therefore it is concluded that the switching losses will be very less as compared with other presented topologies.

3 SWITCHING ANGLE

The switching angles corresponding to the period 0 to $\pi/2$ are called as main switching angles. For N-level inverter, there are (N-1)/2 main switching angles. The two different methods of calculating the main switching angles for the proposed multilevel inverter are given below[15]. Method - 1

$$\theta_i = \frac{i \times 180^\circ}{m} \text{ where, } i = 1, 2, 3, \cdots, \left(\frac{m - 1}{2}\right)$$

$$k = \frac{m + 7}{2}$$  (5)
Method - 2

\[ \theta_i = \sin^{-1}\left(\frac{2i - 1}{m - 1}\right) \text{where, } i = 1, 2, 3, \cdots, \left(\frac{m - 1}{2}\right) \] (7)

where, \( m \) = Number of output levels.

The switching pulses obtained using the method-1 and method-2 are shown in Fig. 5 (a) and Fig. 5 (b) respectively.

Fig. 5. Switching Pulses (a) Method- 1 and (b) Method- 2.

4 SIMULATION RESULTS

To examine the performance of the inverter, the simulation analysis is carried out using MATLAB software. For the analysis, the inverter topology with four voltage sources as shown in Fig. 6 is considered.

Fig. 6. Proposed 9-level topology
The switching states for different output levels is given in Table I. The values of the all sources are equal to 60V i.e., $V_1 = V_2 = V_3 = V_4 = 60\, V$. In this case, the output voltage obtained across the load as 240 V (i.e., $V_1 + V_2$). The 9- level output voltage obtained for different switching methods are shown in Fig. 7. The FFT analysis of the 5-level output voltage waveform is shown in Fig. 8. It is shown that the harmonic content of the output voltage waveform for the switching method - 2 is less when compared with the method-1 and the results are given in Table II.

<table>
<thead>
<tr>
<th>Output Level</th>
<th>Positive Cycle</th>
<th>Negative Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$S_1, S_2$</td>
<td>$S_4, S_3$</td>
</tr>
<tr>
<td>1</td>
<td>$S_3, S_2$</td>
<td>$S_5, S_3$</td>
</tr>
<tr>
<td>2</td>
<td>$S_5, S_2$</td>
<td>$S_6, S_2$</td>
</tr>
<tr>
<td>3</td>
<td>$S_2, S_2$</td>
<td>$S_7, S_2$</td>
</tr>
<tr>
<td>4</td>
<td>$S_4, S_2$</td>
<td>$S_8, S_2$</td>
</tr>
</tbody>
</table>

Fig. 7. Output Voltage (a) Method- 1 and (b) Method- 2.

Fig. 8. FFT Analysis (a) Method- 1 and (b) Method- 2.
5 CONCLUSION

This paper proposed a new symmetric type multilevel inverter with reduced switch count. The main advantage of this inverter is it uses minimum switching components to achieve larger output voltage levels as compared with other presented topologies. The other advantages include simple construction, ease of control, lesser THD and minimum cost. The simulation results during the symmetric operation for 9-level inverter topology is presented. The result shows that the switching angles obtained by method - 2 achieves less THD compared with method - 1.

References


