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A Test Mode Temperature Reduction Technique Based on Dont Care Bit Filling and Fault Dropping

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Abstract

Power density for digital circuits is increasing by the advancement of technology and increased integration. One of the problems is that this dense power dissipation leads to very high temperatures and can affect the correct system behavior. Test mode high switching activity is a fatal contributor to cause IR-drop resulting in increased power density inside the chip.

A true nonessential faults are those faults on which no other faults are dependent and whose removal has no impact on fault coverage but the dropping of such faults contributes significantly to lessen test mode switching activity.

True non essential faults are identified from a list candidate faults and their tracking is very significant considering the fact that these candidate faults make faulty element to switch inside a target region. Care bit positions of the test vectors which are responsible for covering true nonessential faults of a digital circuit, are firstly identified. True nonessential faults are dropped from the coverage by modifying the care bits of the test vectors and thereafter depending on the latest care bit positions, dont care bits are filled by a thermal effect aware x-filling method in order to lower down the extent of switching activity and test mode peak temperature.

***Key Words*:**Thermal effect aware x-filling; true non essential fault; ATPG; IR drop

1 Introduction

Higher chip density and raise in operation frequency has posed several problems of VLSI testing and the test mode high power consumption is one of such problems. Moreover, this highly consumed test power straightway gets transformed into dissipated heat. This high test mode temperature which is elevated test mode by-product is the cause of plentiful staid problems like accelerated failure mechanisms and thermal stress etc. Such overheating of the CUT (circuit under test) may trigger timing errors, permanent damage, overall yield reduction and ultimately making the circuit unreliable. Hence, temperature management during testing is becoming a momentous issue to deal with in the context of testing of VLSI circuits and efficient techniques needs to be evolved in order to control this test mode heat dissipation. We can see several power aware testing strategies in the technical literature which are aiming the reduction of test power. The prime factor of CUTs temperature raise and associated local hotspots formation is the non uniformity in spatial power distribution across the chip and owing to this, reduction of test power alone cannot resolute high temperature related issues cropped up during testing.

This problem caused by IR-drop during VLSI testing further exacerbates the status of defects in an IC and triggers false failures. Lessening of switching activity is necessitated to resolve this issue

and dont care bit filling(X-filling) of the ATPG generated test cube is regarded as one of the effective alternatives to reduce switching-activity by filling the unspecified bits(X-bits) of the test cube. It is revealed from the analysis of relevant literature that over 50% -bits in most of test vectors are X bits. X-filling approach is to keep circuit from transition except target faults by filling X-bits in test vectors. Enokimoto et al. [1] proposed a method to reduce switching activity in critical area. All the surrounding locations nearby the critical path is generally termed as critical area. If switching activity in critical area is higher than a threshold value, the fault is dropped from the test vector in order to reduce switching activity in critical area. A candidate fault is not considered for dropping if it is covered by a single test vector only.

In this paper, based on stuck at fault model, a novel proposal is framed for cutting down test mode temperature. This proposal incorporates a true non essential fault[2] dropping guided X- bit filling algorithm to cut down the extent of test mode switching activity so that IR-drop in hot regions gets lowered down which ultimately contributes to test mode temperature reduction. Our method imports the concept of true nonessential fault which is dropped by modifying the care bits of the test vector. On removal of this fault, switching activity is reduced and thus IR-drop in critical area [2] also gets reduced. In our proposed algorithm, there is no need to add extra test vectors to cover the dropped faults as removal of true non essential is hardly having any impact on fault coverage. The rest of this paper is organized as follows. In Section II, we detail about target vector selection. Section III briefs about the concept of fault dropping Section IV illustrates the dropping of faults from a test cube with the aid of block diagrams and examples results. Section V is detailing all about the application of an existing thermal effect aware x-filling approach on fault dropped test cube and their effects are discussed and analyzed in section VI. Finally, in section VII conclusions are drawn and the direction of future work in this context is shown.

2 TARGET VECTOR SELECTION

Here in this part we describe the process of sorting out such test vector which results in high switching-activity regions (target region). A simplified cost function model known as weighted switching-activity (WSA) [3] is applied to distinguish target regions from other regions. This simplified cost function model delivers a significant increase computational speed. IR-drop in each region is presumed to be independent of each other while computing WSA of any region. The cost function, WSA (region) is defined to represent the IR-drop impact of each region. For a region, it is defined as follows

$$WSA[(block, B_i)] = \sum_{gate}^{\forall gate_i \in B_i} ((1+\alpha Cri_j) \times switching(type_j)) \times \sum_{k \in fanoutofgate_j}^{max} capacitance_k \quad (1)$$

Cri_j represents whether $gate_j$ is on critical path and dened as

$$Cri_j = \begin{cases} 1 & \text{if} \quad gate_i isoncriticalpaths \\ 0 & \quad otherwise \end{cases} \quad (2)$$

Where α is a weight used to emphasize the importance of $gate_j$ if $gate_j$is on the critical path. $Type_j$in Eq. (1) represents type of toggle for$gate_j$. Switching weight of toggle type representing the preference and flexibility to assign specific transition is given in Table.1 bellow

Table.1 Toggle Type of Gates

Toggle Name	Toggle Type	Weight
A	1↔0	2
B	1↔X, X↔0	1.5
C	X↔X	1
D	0↔0, 1↔1	0

For a target vector and a target region, fault removal is performed. Its flow of steps is shown in Fig. 1. We describe each step in detail in following subsections.

A. Care Bit Identification Process

Usually a single test vector covers multiple number of faults of the circuit. Set of faults are covered by setting care bits of the target test vector and these bits must be identified for dropping of faults from the coverage of the vector. Care-bit identification for fault dropping is to identify care-bits for faults covered by the test vector. Care bits which either control the value or propagate value of faults to be observed are identified. Without implementing fault simulation, we use TetraMAX [4] to run fault simulation. We set each care-bit to one by one for the test vector. For each setting, fault simulation is performed. After this step, care-bits corresponding to each individual fault are known. With the information, a fault table is constructed where row and column indices are fault IDs and inputs, respectively. An entry $E_{i,j}$in the fault table f is 1 if the setting of the care-bit in $column_j$ to 1 X-bit will result in the removal of the fault in row_i . Table.2 shows a fault table where there are three faults and five inputs.$fault_1$ is covered when $cbit_1$and $cbit_2$ are set and $fault_2$is covered when $cbit_3$, $cbit_4$ and cbit 5 are set. Similarly,f $ault_3$ is covered when $cbit_2$ and $cbit_4$ is set.

Table.2 Fault Table

	$cbit_1$	$cbit_2$	$cbit_3$	$cbit_4$	$cbit_5$
$fault_1$	1	1	0	0	0
$fault_2$	0	0	1	1	1
$fault_3$	0	1	0	1	1

B. True nonessential faultss

For a test vector and a target region we select candidate faults for fault removal. Candidate fault is defined as covered faults that either are in the target region or propagate through the target region for the test vector. If a fault is covered by more than one test vector then it is here defined as non essential fault. Considering

stuck at fault model, we cannot remove one target fault from the test vector without considering other dependent faults which are on the same sensitized path. This spectrum of non essential fault is further constricted into a more filtered form of fault which was defined as true non essential fault [2]. A non essential fault is called true non essential fault if it does not contribute to other non essential faults and independent of other faults and its propagation paths.

Let row_i represents f aulti in the fault table f as shown in Table 1 and i^{th} care bit,$cbit_i$is $cbit_i = \{col|fe_{i,col} = 1\}$ Then $fault_i$ is known to be true non essential fault [2] if $\{\forall j : cbit_i \cap cbit_j = \varphi\}$ Where j are for each indispensible fault $fault_j$From the fault table shown in Table.2 if we assume that $fault_1$ is indispensible fault and $fault_2$ and f ault3 are ancillary fault. Then,$fault_2$ is a true non essential fault because the care-bits of $fault_2 i.e.cbit_3 cbit_4$ and $cbit_5$ do not intersect with the care- bits of the indispensible fault, $fault_1 i.e.cbit_1$ and $cbit_2$

C. True non essential fault dropping

In this step, we will remove true non essential faults to cut down transition count of a target region without fall in fault coverage. First, we define a feasibility function for the fault elimination in a target region. We assume target fault f_t is covered by the test vector v_i and we define its $removalfeasibility(f_t, v_i) = F_WSA \times \#NoCoverVector$ where F _ WSA is the fall in WSA in the target region when fault f_t is removed from the coverage of a vector v_i and # No Cover Vector is the number of vectors that covers this target fault f t .The more test vectors cover this ft , the less possible the fault coverage drops. A higher$removalfeasibility(f_t, v_i)$ denotes that either this target fault results in large switching-activity reduction in target region or less effect on fault coverage drop after fault removal. We sort these true non essential faults candidates by $removalfeasibility(f_t, v_i)$ and remove fault with the optimum $removalfeasibility(f_t, v_i)$. The removal of true non essential faults [2] carried on until the region has a WSA value less than the threshold value or no true non essential fault can be removed.

3 DROPPING OF FAULT FROM TEST CUBE

Referring to fault table shown in Table 2 it is observed that in case of a genuine ancillary fault,f ault2 we can identify the

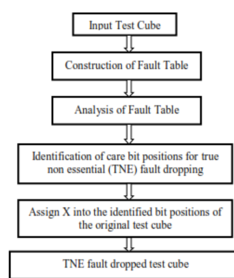

Fig 1: Steps of true non essential fault dropping

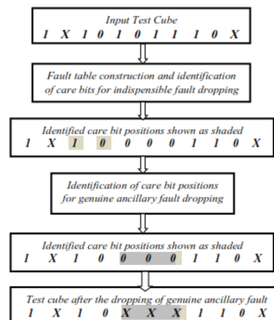

Fig 2: block diagram of true non essential fault dropping

care bit positions which can be set to X by analysing the fault table formulated against a test cube. By the way of setting those respective bit positions to X, it is possible to eliminate those genuine ancillary faults. This is illustrated graphically with following fig. 1

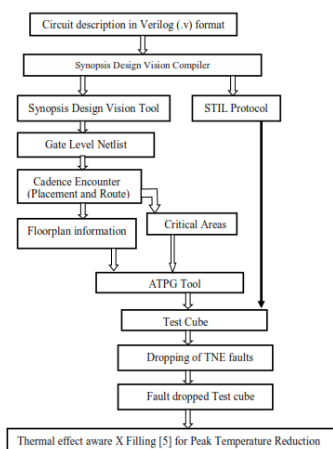

Fig.3 Flow of the Experiment

4 X FILLING OF FAULT DROPPED TEST CUBE FOR TEMPERATURE REDUCTION

Here in this paper our objective is to make the fault dropped test patterns a lot cooler by applying thermal- effect aware don't-care filling technique presented in [5] so that improvement in reduction of peak temperature during testing is achieved. The entire circuit is visualized as numerous blocks of gates and flip flops. Switching elements (like the flip-flops) with high transitions in each block are identified. Floorplan information of the circuit is compulsorily fed to the power estimation tool for estimation of block and thus accommodating the impact of neighboring blocks while estimating the temperature. A thermal effect aware dont care bit (X) filling technique proposed in [5] is applied here on the fault dropped test cube for further boosting the reduction in the test mode peak temperature. Thus peak temperature during testing is further scaled down and controlling of inconsistent temperature distribution across the chip became feasible.

A. Estimation of Power Profile

Estimation of total power for a scan based testing is primarily

focused on the shift power occurring due to the loading and unloading activity inside the scan chains and also switching-in of logic cells during scan shift operation. Switching elements [in short SE] (i.e. flip-flops, scanned flip flops etc.) having a decisive impact on power of a particular block is a major issue of concern in the context of power estimation.

As a block may consist of several SEs, so the extent of switching activity has got a significant role in determining power totality of that respective block. As stated earlier, higher switching activity in switching elements(SE) results in higher power consumption in that respective block. So, we include these neighboring contributors SEs (i.e., flip-flops) with the native SEs of the block and define them as power decisive elements (PDE) for that block. The metric for estimating total power of a CUT is formulated in [5] as t ot alnumberofblocks

$$P = \sum_{i=0} P_{dec} \tag{3}$$

P_{dec}, corresponds to power decisiveness [5] of block Bi may be expressed by the following equation in [5]:

$$r_{dec} = \frac{PB_{tn}}{P_{pde}} \tag{4}$$

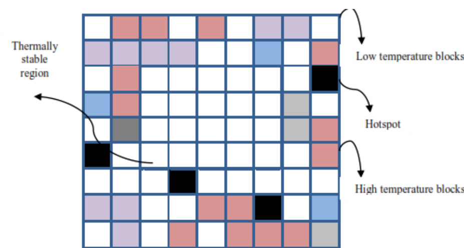

Fig 4 Temperature blocks in a region

B. Derivation of temperature profile from the power profile and floorplan information

Fig. 4 shows the partition of a CUT into 99 equally sized blocks. The color of each block reflects the thermal profile of the block during testing (dark colors means high temperatures).If two regions are geometrically in close proximity to each other, then a large thermal

gradient drives considerable heat flow between them which results in speedy temperature change. As a result, necessity for thermally stable regions arises which can absorb heat from this region and other neighboring regions that develop high temperatures. Since bulk of the test power dissipation occurs during scan-in process, the transitions occurring inside the thermally stable regions during this process must be minimized.

Analysis of high switching-activity identifies a target region corresponding to a test vector. Target regions are differentiated from other regions with the aid of an amended cost functionweighted switching-activity (WSA) [3]. The parameter temperature criticality, denoted as T critical in [5] is defined to determine how muck hot a block may turn into all through testing. Temperature criticality, T critical for a particular block B i, is derived by computing the power (P) cost average of the qualified direct-contact- adjacent-blocks. Quantity of power consumed by a block and underlying topology of corresponding and the adjacent block derives the temperature of each block. Power consumed by block i , is denoted as Pi and temperature of block i is represented as Ti and m number of blocks are considered. The tool Hotspot can produce the transfer thermal resistance matrix if the oorplan for a set of blocks is given .A model with the following assumptions is applied in a dynamic architectural power simulation by inputting dynamic values to the tool, Hot Spot for computing block wise power density and corresponding temperature of each block. Hot Spot 6.0 is used for performing thermal simulations in order to get the stable state profile of the chip under test. The tool Hotspot [6, 7] is well-known for its thermal modeling speed and accuracy. It is applied for the assessment of the maximum temperature among all the blocks in the oorplan. Temperature trace is derived from the oorplan file and power trace file. In the following section, we give a brief overview of the steps involved in carrying out temperature simulation

In this approach our motive is to lesser down the frequency of hotspot creation by reducing the highly intense power consuming areas through thermal effect aware [5] dont care bit filling of the fault dropped test set. Temperature findings provided in the Table 5 and Table 6 of the experimental outcomes and analysis section are derived from Hotspot tool.

C. Overview of Temperture Simulation

1. Circuit description in Verilog format (.v) is taken as input & compilation of the design was done by Synopsys Design Vision logic synthesis tool [8] and synthesized using the Synopsys Design Vision Compiler [8] to generate a gate level netlist.

2. Synopsys DFT Compiler is used for replacement of all the ordinary flip flops by scanned flip flops.

3. Floorplan is obtained with the aid of a Cadence tool namely Encounter [9] .A scan inserted design description is fed as input to the tool and a standard cell library is also accessed in order to extract floorplan information.

4. Scan inserted netlist, and the test patterns are inputted to a power profile estimation tool. The estimation of power consumption against each of the switching elements (i.e. gate, flip-flop) is done for different inputs by using the Synopsys Design Vision tool and stored in a database. These stored values of transitions in individual logic elements is converted to their corresponding power profile values during circuit simulation for each scan shift and capture cycle.

5. Floorplan is divided into the equal sized blocks for thermal simulation and block wise power profile values are calculated.

6. Thermal simulator Hot Spot 6.0 [6] is used for getting the temperature distribution. Pre computed power profile and block-level floor plan is supplied as input to the thermal simulator for getting the results.

Table 3: Reduction in percentage of power variance, average power and maximum power by the approach in [5]

Circuit	Random Filling			MT Filling			1- Filling			0-Filling			BSCO [10]		
	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}
b12	77.1	7.8	16.6	87.3	- 29.9	- 0.9	89.4	- 29.2	3.4	89.0	- 29.7	3.3	85.72	-21.37	3.51
b14	53.5	17.3	18.1	53.9	- 40.1	5.8	60.7	- 27.9	7.2	54.9	-37.2	1.5	46.93	-26.20	2.74
b15	80.9	21.5	9.0	42.1	- 59.1	- 6.2	49.6	- 53.2	0.4	37.7	-69.4	-2.1	49.43	-45.23	-1.67
b17	88.3	35.4	9.1	89.5	- 63.2	- 3.6	87.8	- 58.8	- 5.7	90.1	-57.6	-2.7	87.52	-43.21	-1.72
b20	65.7	16.2	14.3	67.6	- 27.1	- 3.0	76.3	- 17.1	3.2	69.7	- 14.8	1.1	68.14	-8.90	1.39
b21	49.7	15.7	-0.5	59.1	- 26.0	- 11.9	62.1	- 18.2	- 11.4	67.2	-26.5	-9.4	67.25	-17.23	-4.95
b22	67.4	19.9	7.7	78.8	- 25.6	-4.4	81.1	- 12.5	-1.6	83.3	-19.3	0.8	75.82	-17.82	1.76
Ave	68.89	19.11	10.61	68.33	- 38.71	- 3.46	72.43	-30.99	- 0.64	70.27	-36.36	-1.07	68.69	-25.70	0.15

Table 4: Reduction in percentage of power variance, average power and maximum power after fault dropping

Circuit	Random Filling			MT Filling			1- Filling			0-Filling			BSCO [10]		
	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}	ΔP_{spv}	ΔP_{ave}	ΔP_{high}
b12	78.2	8.9	18.4	86.1	- 24.6	- 0.2	87.2	- 19.8	3.9	87.3	- 23.7	5.2	85.32	-16.30	5.11
b14	55.9	16.8	22.4	57.5	- 31.6	9.8	66.3	- 28.4	10.0	59.7	-28.2	2.7	48.23	-21.40	3.24
b15	84.3	25.9	11.2	46.4	- 47.2	- 3.4	48.2	- 46.5	2.5	48.6	-59.3	-1.2	50.94	-37.19	1.07
b17	87.2	34.4	9.2	87.8	- 54.2	- 1.5	86.8	- 49.1	- 2.7	88.3	-49.4	-1.8	86.92	-35.43	-1.12
b20	67.7	19.2	17.7	69.8	- 18.9	- 1.8	78.9	- 14.3	2.7	68.2	- 10.3	2.4	69.91	-5.71	2.19
b21	49.3	16.7	1.8	64.9	- 17.1	- 7.1	67.5	- 12.1	- 8.9	69.8	-17.5	-5.5	68.89	-12.33	-2.15
b22	71.1	19.3	8.7	77.2	- 21.8	-2.3	85.2	- 14.5	2.2	86.7	-14.6	1.8	77.32	-15.94	-0.77
Ave	70.52	20.17	12.77	69.96	- 30.77	- 0.93	74.30	-26.38	1.64	72.66	-29.00	0.51	69.65	-20.61	1.08

Table 5: Percentage of reduction in temperature divergence and peak temperature by the method in [5]

Circuit	Random Filling		MT Filling		1- Filling		0-Filling		BSCO [10]	
	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}
b12	88.9	13.6	92.9	- 2.3	95.2	0.9	95.7	- 2.8	89.12	- 1.55
b14	66.2	12.8	61.1	- 11.8	67.1	- 5.5	60.7	- 7.9	65.76	- 8.93
b15	74.5	13.7	48.7	- 8.5	57.4	- 9.7	38.8	- 18.2	47.30	- 7.2
b17	87.1	28.0	76.1	- 12.1	78.8	- 9.7	78.1	- 8.7	78.61	- 10.06
b20	65.4	14.6	52.3	- 8.9	68.1	- 3.1	59.6	- 1.7	56.32	- 9.02
b21	47.3	9.4	56.3	- 9.3	59.1	- 5.8	65.3	- 6.7	59.91	- 6.4
b22	56.9	15.8	63.6	-5.4	73.2	-0.5	58.9	- 0.8	67.80	1.40
Ave	69.47	15.41	64.43	-8.33	71.27	-4.77	65.2	- 6.69	66.40	-7.16

Table 6: Percentage of reduction in temperature divergence and peak temperature after fault dropping

Circuit	Random Filling		MT Filling		1- Filling		0-Filling		BSCO [10]	
	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}	$\Delta T_{divergence}$	ΔT_{peak}
b12	89.12	18.11	88.15	- 0.91	88.21	01.48	90.22	03.28	87.81	01.32
b14	63.34	16.12	67.91	- 7.18	75.25	- 03.52	65.02	- 03.95	66.86	- 06.29
b15	77.05	15.75	56.37	- 4.52	56.49	- 04.12	45.90	- 14.21	47.39	- 05.12
b17	86.78	27.96	75.12	- 6.11	85.80	- 10.19	77.16	- 05.77	78.91	- 06.15
b20	67.39	16.84	57.83	- 7.82	77.12	- 00.91	63.74	02.32	58.92	- 05.72
b21	49.20	08.89	58.09	- 5.00	79.41	- 01.74	67.40	- 03.17	59.45	- 03.48
b22	59.10	18.17	67.50	1.14	78.15	02.28	59.33	01..89	69.51	02.14
Ave	70.28	17.33	67.28	-4.67	77.20	-02.39	66.97	-02.80	66.97	-03.33

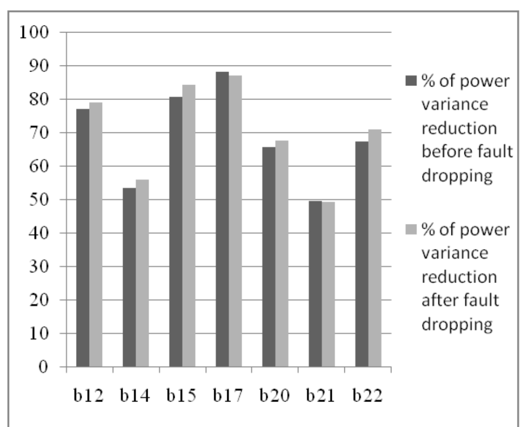

Fig.5: Fault dropping effect on power variance reduction % for random fill

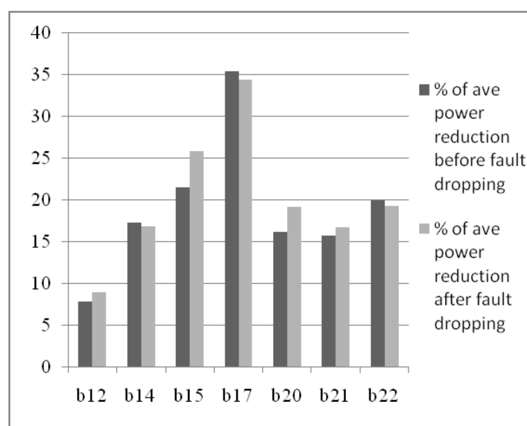

Fig.6: Effect of fault dropping on ave. power reduction % for random fill

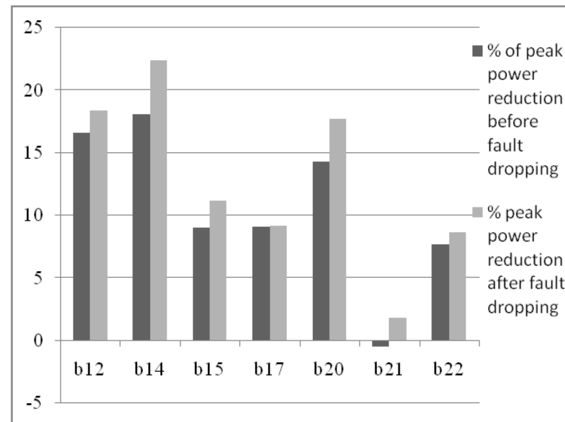

Fig 7: Fault dropping effect on peak power reduction % for random fill

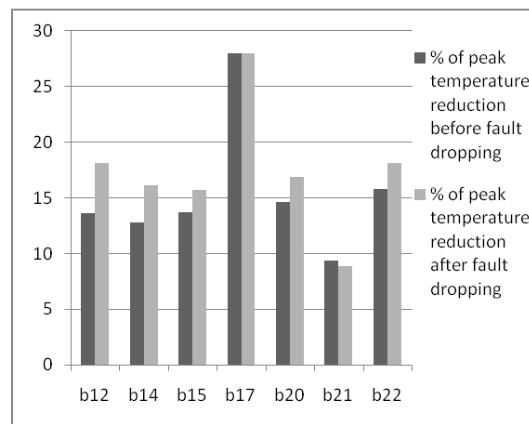

Fig 8: Fault dropping effect on peak temperature reduction % for random fill

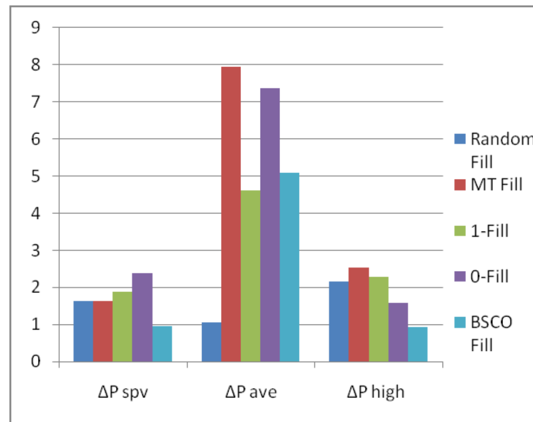

Fig 9. Improvement in the average reduction % of spatial power variance (Pspv,) average power (Pave) & maximum (peak) power(P high)corresponding to different filling methods

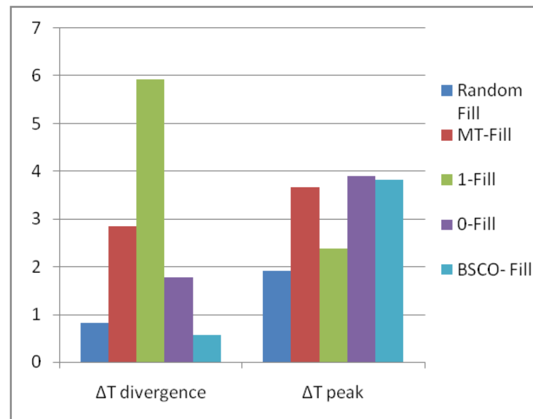

Fig 10. Improvement in the average reduction % of temperature divergence (T divergence) & peak temperature(T peak) corresponding to different filling methods

5 EXPERIMENTAL OUTCOMES AND ANALYSIS

Experimentation was carried out on the selected ITC99 benchmark circuits. Synopsis Tetramax [4] ATPG tool with the assumption of

stuck-at fault model was applied to generate test cubes corresponding to the ITC99 benchmark circuits. The thermal effect aware x filling approach referred in this paper for manifestation of the effect of dropping of true non essential faults from the test cube, bears a significant impact on the block level power consumption and temperature and owing to this, reporting of both the profiles in each of the following filling cases namely 0-fill (X-bit is filled by 0), 1-fill (X-bit is filled by 1), MT-fill (To get minimum number of scan transitions) ,random-fill (X-bits are filled up randomly) and BSCO fill[10] ,became noteworthy.

The relative difference in the power variance (ΔP_{spy},), average power (ΔP_{ave}) and maximum power(ΔP_{high}) between the referred thermal effect aware x filling approach and existing approaches namely 0-fill, 1-fill ,MT-fill, random-fill and BSCO fill is focused here. The relative difference in the spatial power variance (ΔP_{spy}) is derived by the equation (1)

$$\Delta P_{spy} = \frac{P - P_{TXF}}{P_{existing}} \times 100 \tag{5}$$

Where $P_{existing}$ and P_{TXF} denotes the power variance exhibited by the existing X filling approaches like 0-fill, 1-fill etc. and referred thermal effect aware x filling method respectively. So other similar parameters emphasizing relative difference can be computed in a similar fashion.

The outcomes of thermal effect aware x filling approach [5] in terms of reduction in % of power variance (ΔP_{spy},), average power (ΔP_{ave})and maximum power(ΔP_{high}) against different filling methods, is shown in Table 3 and the experimental outcomes tabulated in Table 4, describes the effect of applying fault dropped test data set as input to the thermal effect aware x filling approach. In Table 4, it is found that the output parameters like reduction in % of power variance, average power and maximum power against different filling methods has shown significant improvement with respect to those of Table 3 in most of the cases. A graphical comparison of the output parameters namely reduction in % of power variance, average power and maximum power before and after the application of fault dropped test cube against random x- filling method is shown in the Fig 5 to Fig 7

Table 5 shows the details of percentage of reduction in tempera-

ture divergence and peak temperature with respect to different filling techniques against the thermal effect aware approach referred in this paper. Thermal simulation of the ITC99 circuits using the tool HotSpot 6.0 was done in order to generate the temperature profile. ΔTdivergence denotes the difference in the temperature divergence between the referred thermal effect aware x filling approach and corresponding five different filling techniques Table 6 details about the percentage of reduction in temperature divergence and peak temperature when a fault dropped test cube is chosen as input to thermal effect aware x filling and almost in all the cases significant performance improvement is recorded. Fig 8 shows a graphical comparison of reduction in peak temperature before and after the application of fault dropped test cube corresponding to random x-filling approach. In Fig 9, performance enhancements in respect of average reduction % of spatial power variance (ΔP_{spy},) average power (Pave) and maximum (peak) power(ΔP_{high}) corresponding to different filling methods, are projected graphically through bar graph.

Fig 10, graphically represents the improvements in the average reduction % of temperature divergence (T divergence) and peak temperature (T peak) corresponding to different filling methods.

6 CONCLUSION AND FUTURE WORK

The idea of utilizing the concept of dropping the true non essential faults from a test cube before feeding it to thermal effect aware x filling approach is a novel one. This facilitates the two fold reduction in switching activity: firstly, through the process of fault dropping and lastly but not the least, with the aid of thermal effect aware x filling thereby reducing the overall power dissipation during testing. The initial result of power profile computation reveals the efficacy of this scheme and also reflects the suitability of importing the concept of fault dropping into the problem domain of test mode temperature reduction. Thermal profile computation confirms the significant performance enhancement with respect to existing thermal effect aware x filling approach. However due to the obviousness of care bit manipulation for dropping of true non essential faults from the test cube, fault coverage towards some un-

modelled faults may get affected and further research for extending solvable measures in this regard may contribute significantly to the robustness of this approach.

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