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# Comparative Analysis of Novel 9T Static Random Access Memory at different technologies of FinFET

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**Abstract**

The demand on the design of Static Random Access (SRAM) is been increasing with the advancement in CMOS technology. In this paper, novel 9T SRAM cell is implemented using FinFETs at two different technologies that is 18nm and 7nm using Cadence software. The proposed design uses power gating technique to decrease the leakage power dissipation. The stability is analyzed using N-curve analysis method. The results show that the memory cell implemented in 7nm shows improvement of 60.18% in write ability, 75.33% less leakage power than the same memory cell designed in 18nm.

***Key Words*:**N-curve, low leakage power, FinFETs, SRAM

## 1 Introduction

Memory is one of the important component of any digital system and due to this static random access memory (SRAM) performance

will influence the performance of the system to a greater extent. The astounding growth in technology has created the need to design low power SRAM cells. The amount of leakage power in total power dissipation is also increasing with technology node [1]. Fin shaped Field Effect transistors (FinFET) is the best known replacement for the conventional Metal Oxide Semiconductor Field Effect Transistor(MOSFET) as it shows less leakage power dissipation due to its better control over short channel effects(SCE) that are majorly responsible for leakage power. The leakage power of SRAM cell must be decreased by maintaining the stability of the SRAM cell. The stability of the conventional 6T SRAM cell decreases to unacceptable level due to the degradation in the supply voltage. Recently novel designs are proposed in [2] and [3] and these designs shows less leakage power dissipation along with increase in the stability factors by using more number of transistors but this gives an area overhead. The proposed design uses less number of transistors and also will decrease the leakage power dissipation and increase the stability factors such as read stability, write ability and access times.

# 2 PROPOSED 9T SRAM CELL DESIGNS

The proposed design uses single ended schemes for both write and read operation and this will considerable save power in read and write operation since most of the power is wasted in charging and discharging both the bit-lines in double end schemes. The schematic of proposed design implemented using FinFET 18nm and 7nm in cadence virtuoso tool is shown in Fig. 1. and Fig. 2.

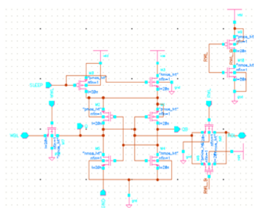

Fig.1. Schematic of proposed design in 18nm

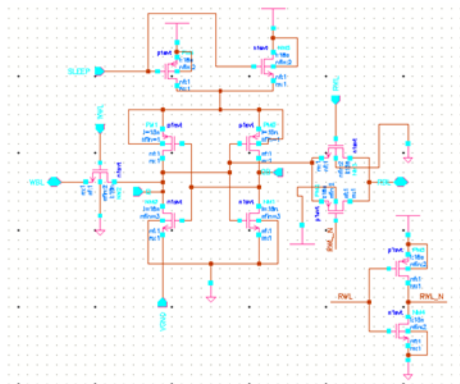

Fig. 2. Schematic of proposed design in 7nm.

It is already a known fact that writing 1 into the memory cell that utilizes single-end scheme is difficult as the said operation is achieved by pulling another node to 0 in double end schemes. To facilitate the operation, one of the pull down transistors ground is made floating with the help of virtual ground (VGND) pin so that write 1 operation can be done easily. Power gating technique is applied wherein the circuit connects to full power supply only for write and read operations and for idle operation the circuit connects to half of the power supply. This will save considerable amount of power in hold operation. There are two different control signals write word line (WWL) and read word line (RWL) that are responsible for read and write operation respectively. WBL represents the write bit-line and RBL represents the read operation. The condition of control signals in read, write and hold operation is shown in table I.

TABLE I. OPERATION TABLE OF PROPOSED MEMORY CELL

| Signal | Hold | Read | Write |
|---|---|---|---|
| WBL | -- | -- | VDD/GND |
| WWL | GND | GND | VDD |
| RWL | GND | VDD | GND |
| VGND | GND | GND | FLOAT |
| SLEEP | VDD | GND | GND |

As tabulated in the table, For Write operation, the data to be written inside the memory cell will be placed on the WBL and then the WWL signal will be made high. To make the write operation easy, VGND pin will be floating and to connect the circuit to full power supply, the SLEEP control signal will be grounded.

For read operation, the WWL will be made low and RWL signal will be asserted high. The data present inside is read and will be present at RBL. VGND will be connected to ground and SLEEP control signal will also be grounded for the correct operation.

For Hold operation, both WWL and RWL signal will be grounded and SLEEP control signal will be asserted high so that the circuit connects to half of the power supply and this saves most of the power dissipation.

# 3 SIMULATION SETUP

The proposed design is implemented and simulated for its functionality verification using Cadence Virtuoso tool. As explained before, the designs are implemented using 18nm and 7nm FinFET technologies. The different performance parameters that are considered for performance evaluation are read and write stability, read and write access time, read and write power, leakage power.

*A. Read and Write Stability*

The stability of SRAM is decided by the static noise margin (SNM). This Static noise margin is conventionally measured using butterfly curve [4]. It is already known fact that the stability information can be extracted even more efficiently than butterfly curve using N-curve Analysis [5]. Thus, N-curve analysis is used to measure the stability of the proposed cell. *B. Read and Write Access time*

The time taken by the bit-line that is responsible for the read operation to attain a atble state that will indicate the stored data upon activation of the control signal responsible for the read operation can be termed as read access time. Similarly, the time taken by the output node to indicate the value that is placed on the bit-line responsible for write operation upon activation of the control signal that is responsible for the write operation can be termed as write access time.

*C. Read and Write Power*

The power consumed for correct read and write operation is known as read and write power dissipation respectively. This power includes the power needed for floating the VGND control signal for write operation.

*D. Leakage Power*

In SRAM cell, the major source of leakage power is the cross coupled inverter that helps in storing the data. In the proposed design, power gating strategy used to decrease the leakage power consumption.

# 4 RESULTS

Fig. 3. Shows the read, write and hold operation of the proposed design simulated in Cadence tool.

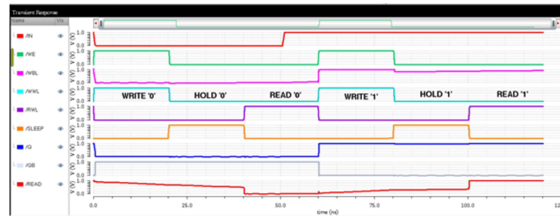


Fig. 3. Write, Read and Hold Operations in the proposed memory design.

As shown in the Fig. 3., all the operation can be done successfully in the proposed scheme. To validate the performance of the proposed cell, the design is compared with the SRAM cell designs proposed in [2] and [3]. To make a thorough comparison, designs in [2] and [3] are also implemented using FinFET 18nm technology and performance values are computed for the same. Table 2 shows the comparison between the proposed cells and the designs proposed in [2] and [3].

TABLE II. PERFORMANCE PARAMETERS COMPARISON OF SRAM CELLS

| Performance Parameter | ST2 [2] | ST3 [3] | Prop. Novel 9T cell in 18nm | Prop. Novel 9T cell in 7nm |
|---|---|---|---|---|
| *SPNM in μW* | 5.845 | 8.622 | 7.55 | 7.53 |
| *WTP in μW* | -6.005 | -5.993 | -7.318 | -11.722 |
| *RA '0' in ps* | 6.902 | 18.39 | 20.44 | 15.83 |
| *RA '1' in ps* | 25.74 | 71.65 | 15.35 | 7.27 |
| *WA '0' in ps* | 111.3 | 98.31 | 82.52 | 14.67 |
| *WA '1' in ps* | 104 | 201.4 | 119.5 | 78.51 |
| *RP '0' in Nw* | 2464 | 148 | 162.3 | 48 |
| *RP '1' in Nw* | 44.92 | 86.48 | 63.84 | 53.9 |
| *WP '0' in Nw* | 110.8 | 133.7 | 110.2 | 15.41 |
| *WP'1' in Nw* | 85.69 | 184 | 89.57 | 56.32 |
| *Leakage Power in μW* | 10.25 | 11.72 | 3.26 | 0.804 |

**RA: READ ACCESS TIME, WA: WRITE ACCESS TIME, RP: READ POWER, WP: WRITE POWER**

For a cell to be stable Static Power Noise Margin (SPNM) should be positive and will quantify the read stability and Write trip power(WTP) should be negative [5] and it quantifies the write ability. It is said that the cell with high SPNM and low WTP has more stability. From table II, it can be observed that though the proposed design has 12.4% less read stability than [3] but if write ability is considered then there is 22.11% and 95.6% improvement when the proposed design is implemented in 18nm and 7nm respectively. The proposed designs occupying less area are able to be as robust as that of designs in [2] and [3]. The proposed design implemented in 18nm shows considerable reduction in power consumption for read and write operation. It can be observed that proposed design implemented in 7nm consumes only 1.9%, 32.43% and 13.9%, 11.52% of power for read and write operation of logic 0 when compared with [2] and [3] respectively. If leakage power is taken into consideration, then the proposed design in 7nm dissipates only 7.84% and 6.8% power when compared to [2] and [3].

# 5 CONCLUSION

A robust single-ended 9T SRAM cell is proposed and is tested for its functionality in Cadence Virtuoso tool. Further, the performance parameters are computed and are compared with the recent designs. It is observed that the proposed design shows 22.11% and 95.6% improvement in write ability in 18nm and 7nm respectively when compared with [3], dissipates only 31.8%, 7.84% and 27.81%, 6.8% of leakage power when compared with the recent design in [2] and [3] respectively. It can be concluded that the proposed designed while maintaining the good stability factors, dissipate less leakage power and also will occupy less area.

# 6 FUTURE SCOPE

There is a very large scope for further reduction of power. Low power strategies and FinFET transistors that have low threshold

voltage can also be used to reduce power. Other device families such as pseudo NMOS or dynamic logic can also be used to reduce the power consumption.

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