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# A NEW SINGLE PHASE BRIDGELESS AC/DC POWER FACTOR CORRECTION USING SEPIC

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**Abstract**

This paper proposes a new single phase bridgeless AC/DC power factor correction (PFC) topology using SEPIC converter to improve the power factor due to non-linear loads connected and by reducing total harmonic distortion (THD) of the utility grid. By eliminating the input bridge in conventional PFC converters, the control circuit is simplified. The controller operates in multi loop fashion as the outer control loop calculates the reference current through innovative filtering and signal processing. Inner current loop generates PWM switching signals through the PI controller. Performance of the proposed PFC topology is verified using PSIM circuit simulations.

***Key Words***:Bridgeless SEPIC converter, PFC, Multi loop control.

# 1 INTRODUCTION

In recent years the demand for improving the power quality of ac system has become great concern due to increased number of electronic equipments. Todays commercial, industrial, retail and even domestic premises are increasingly populated by electronic devices such as PCs, monitors, servers and photocopiers which are usually powered by switched mode power supplies(SMPS). Harmonics can damage cabling and equipment within this network, as well as other equipment connected to it. Problems include overheating and fire risk, high voltages and circulating current, equipment malfunctions and component failure, and other possible consequences [1][2]. A non-linear load is liable to generate these harmonics if it has poor power factor.

In order to ensure good quality power supply various international agencies have proposed different standards such as IEC 1000-3-2, EN 61000-3-2, IEEE 519-

1992 etc. These standards give practices and requirements for harmonic control in electrical power system for both individual consumers and utilities [4]. So to comply with recommended standards it is necessary to use suitable power factor correction technique to reduce the harmonic distortion in power lines and improve the power factor PFC research became an active topic in

Power electronics and significant efforts have been made on the developments of the PFC converters. As a matter of fact, the PFC circuits are becoming mandatory on single phase power supplies as more stringent power quality regulations and strict limits on the total harmonic distortion (THD) of input current are imposed. With purely resistive loads, the voltage and current waveforms are exactly in phase and the power factor is exactly 1 (unity), however a wide range of industrial equipment such as motors, transformers and even fluorescent lights draw some element of inductive current. This is the current needed to establish the magnetic field required for these items. All magnetic fields require inductive currents lagging their voltages by 90so the resulting overall current is no longer

in phase with its voltage.

The active power (expressed in kW) is therefore less than the apparent power (expressed in kVA). The apparent power is the victories sum of the active power and the reactive power (expressed in kVR). In order to correct for the inductive load, capacitors can be added to the system. With a capacitor, the current leads the voltage instead of lagging behind it. Therefore, the effect of the capacitive load can be used to compensate for the effect of the inductive load, reducing the overall reactive load. In reality, the inductive and capacitive currents both continue to flow, but the power flows

from the inductive load to the capacitive load and back. Therefore the utility is no longer needed to supply the reactive current, so the current flowing in the utilitys distribution system is reduced. Power supplies with active power factor correction techniques are becoming increasingly popular for many types of electronic equipment to meet harmonic regulations and standards [3-7]. In active PFC an active switch are used in conjunction with reactive elements and provides more efficient solution for power factor correction. Also the output voltage is controllable. In active power factor correction the switching takes place at high frequency and shapes the input current as close as possible to a sinusoidal waveform which is in phase with input voltage. The drawbacks are dc output voltage is always higher than the peak input voltage, inputoutput isolation cannot be easily implemented, high start up inrush current, as well as a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents [2].

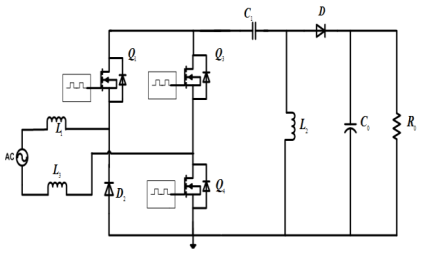


Fig.1. Proposed Diagram for Bridgeless SEPIC PFC

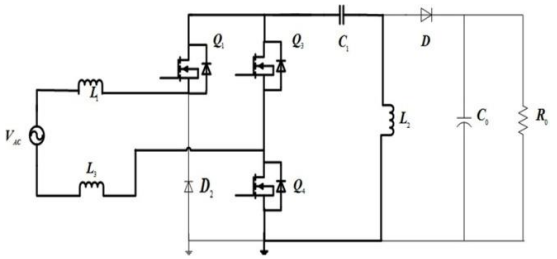

Fig.2. Proposed SEPIC PFC for mode 1

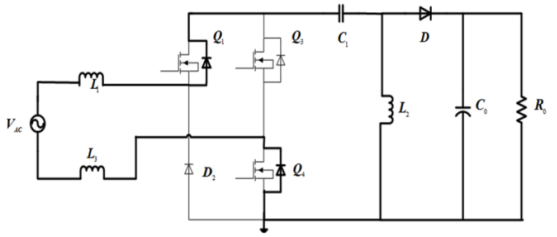

Fig.3. Proposed SEPIC PFC for mode 2

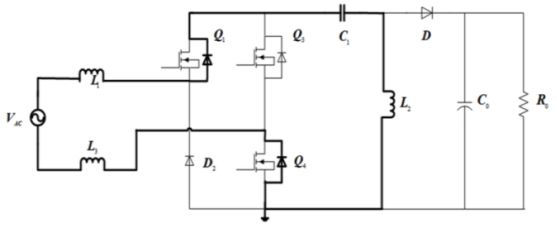

Fig.4. Proposed SEPIC PFC for mode 3

The proposed bridgeless SEPIC PFC converter with three active switches is shown in Fig1. Three switches $Q\_1$ , $Q_3$ and $Q_4$ turn on, when the input inductor currents start to increase linearly. The outputinductor voltage is equal to the voltage of $C_1$ which was equal input voltage before the switches are turned on. Thereby, $i_{L2}$ reduces linearly. This mode finishes by turning off $Q_1$ , $Q_3$ and $Q_4$ . By turning $Q_1$, $Q_3$ off, D starts to conduct. Input inductorcurrent reduces linearly and $i_L2$ increases linearly until the diode current extinguishes.When D turns off, output side is disengaged from the input side, the current through the inductors freewheel at the input side. Working modes for proposed SEPIC PFC converter are below.

# 2 PRINCIPLE OF OPERATION

The proposed SEPIC converter circuit comprises of two symmetrical structures and the circuit is investigated for the positive half cycle structure. Suggesting that the circuit working in a positive half cycle of a switching period Ts can be divided into three working modes, and it can be defined as follows.

Mode 1: In this mode, $Q_1$, $Q_3$ and $Q_4$ switches are turned on, as shown in Fig 2. In this mode, the input inductor currents increase and output inductor current decreases linearly at a rate proportional to the input voltage $V_ac$. Three switchesconducted at this time to charge the input inductors. The rate of increase of the input inductor currents and the rate of decrease of output inductor current are given by

$$\frac{di_{ac}}{dt} = \frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = \frac{V_{ac}}{L_{1,3}} \tag{1}$$

$$\frac{di_{ac}}{dt} = \frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = \frac{V_{ac}}{L_{1,3}} \tag{2}$$

Where $L_{1,3}$ values is given by,

$$\frac{1}{L_{1,3}} = \frac{1}{L_1} + \frac{1}{L_3} \tag{3}$$

Thus, the switch current is given by

$$i_{Q3} = i_{ac} - I_{L2} = \frac{V_{ac}}{L_{1,3}} + \frac{V_{ac}}{L_2} \tag{4}$$

This mode ends when $Q_1$, $Q_3$ and $Q_4$ switches are turned off, starting the next mode.

Mode 2: In this mode, $Q_1$, $Q_3$ and $Q_4$ switches are turned off as shown in fig 3.But $Q_1$ and $Q_4$ are conducting through anti parallel body diodes. Fast diode D is turned on, providing a route for the input and output inductor currents. In this mode, the input inductor currents decrease linearly at a rate that is proportional to the output voltage $V_dc$ and output inductor current increase linearly. The three inductor currents are given by

$$\frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = -\frac{V_{dc}}{L_{1,3}} \tag{5}$$

$$\frac{di_{L2}}{dt} = -\frac{V_{dc}}{L_2} \tag{6}$$

This mode ends when the diode current distinguishes. Mode 3: In this mode, all the active switches are turned off, as shown in Fig4. $Q_1$ and $Q_4$ are conducting through anti parallel body diodes. This mode ends by starting the next switching cycle. In this mode, the inductors $L_1$, $L_2$ and $L_3$ currents are equal. The switch voltage and diode voltage are equal input voltage $V_{ac}$ and output voltage $V_{dc}$ respectively. The duration of this mode is

$$\Delta_1 = \frac{V_{ac}}{V_{dc}} * d \tag{7}$$

Where d is the duty cycle.

# 3 COMPONENT SELECTION AND SIMULATION RESULTS

The standard design equations for the main components of the AC/DC SEPIC PFC converter are provided [4-7]. The proposed converter is designed for $20V_rms$ 50 Hz AC input voltage to generate at 10 V DC. The input current ripple is limited to 20% of the peak current I ac_peak with the switching frequency f_s of 30 KHz.

The following calculations are used to select the appropriate inductors for $L_1$ and $L_2$. For an approximate efficiency $\eta$ of 95%, following equation can be derived,

$$I_{ac} = I_{acpeak} sin(\omega t) = \frac{2 \times \pi}{\eta \times V_{acpeak} \times sin(\omega t)} \tag{8}$$

$$I_acpeak = 140mA \tag{9}$$

Input current ripple is

$$\Delta I_L = 20\% I_{acpeak} = 28mA \tag{10}$$

$$\Delta I_L = \frac{V_s \times d}{L_1 \times f_s} \tag{11}$$

The output current in a switching period is equal to the average of the fast diode current. The output average current switching period is obtained by

$$i_{dc_avg} = 0.5 i_{dc\_peak} \Delta_1 \tag{12}$$

Where, $i_{dc_avg}$ the peak current of fast diode and $\Delta_1$ is the duty ratio of D,$\Delta_1(1-d)$ and $i_{dc_avg}$ can be calculated as:

$$i_{dc_peak} = i_{L1} + i_{L2} = \left(\frac{1}{L_{1,3}} + \frac{1}{L_2}\right) V_{ac} d_{Ts} \tag{13}$$

$$i_{dcavg} = 0.5 \left(\frac{V_{ac}^2}{\left(\frac{1}{L_{1,3}} + \frac{1}{L_2}\right) V_{dc}}\right) d^2 T_s \tag{14}$$

$$i_{dcavg} = (\frac{1}{\pi}) \int_0^{\pi} i_{dc_{avg}} d\omega t = \frac{V_{ac(peak)}^2}{4 L_{eV} dc} d^2 T_s \tag{15}$$

Where,

$$L_e = \frac{L_{1,3} \times L_2}{L_{1,3} + L_2}$$

From (11), the duty cycle d is calculated as:

$$d < \frac{V_{dc}}{V_{ac} + V_{dc}} = 0.22 \tag{16}$$

Selecting d = 0.2, we would get

$$L_e = \frac{V_{acpeak}^2 \times d^2}{4 V_{dc} f_s \times I_{dcavg}} = 180 \mu H \tag{17}$$

$L_1$ and $L_3$ can be obtained as

$$L_{1,3} = \frac{V_{acpeak}^2 \times d}{f_s \times \Delta I_L} = 180 \mu H \tag{18}$$

$$L_1 = L_3 = \frac{L_{1,3}}{2} 180 \mu H \tag{19}$$

Therefore, $L_2$ can be obtained from the following equation

$$\frac{1}{L_2} = \frac{1}{L_e} = \frac{1}{L_{1,3}} = L_2 = 100 \mu H \tag{20}$$

The output capacitance needed to achieve desired current ripple can be calculated as

$$\frac{P_{load}}{V_{dc} \times \Delta V_{dc}(\%) \times 4 \times f_{ac}} = 2.2mF \tag{21}$$

To verify the validity of the proposed SEPIC PFC converter, well known software PSIM software is adopted and carried out the simulation process. The simulation parameter of the proposed SEPIC PFC converter is tabulated below

Table.1. COMPONENTS OF PROPOSED SEPIC PFC

| PARAMETER | PROPOSED SEPIC |
|---|---|
| Switching frequency | 30KHz |
| Inductors L3<br>L2<br>L1 | 100µH<br>4.4mH<br>4.4Mh |
| Capacitors C1 | 0.135µF<br>2.2mF |
| R Load | 10Ω |
| PI (Gain values) | 0.01<br>0.04 |

The multi loop control is proposed for the converter, outer voltage controller generating the reference current to regulate the DC voltage and the inner PI controller generating the gating signals as shown in Fig 4. The high frequency switching of the converter produces switching ripples on the DC voltage. Thus the measured DC voltage is processed through a band stop filter to eliminate the noise on the measurements.

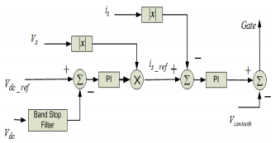


Fig.4. Block diagram of controller

Fig 5, presents the proposed circuit of bridgeless SEPIC PFC converter. The proposed bridgeless SEPIC topology is simulated to compare with conventional SEPIC. PSIM simulation software was used to verify the steady state waveforms of each component. The proposed converter is designed for 20 $V_rms$; 50 Hz AC input voltage to generate at 10 V DC. The input current ripple is limited to 20% of the peak current ac peak current with the switching frequency $f_s$ of 30 KHz .The duty ratio reference was selected as 0.34 which corresponds the required duty reference to produce 10V output at the peak of the input voltage and two PI controllers with gain values of 0.01 and 0.04 is given. The 2nd order band stop filter gain, centre frequency and stopping band are designed as 1,120 and 20 respectively.

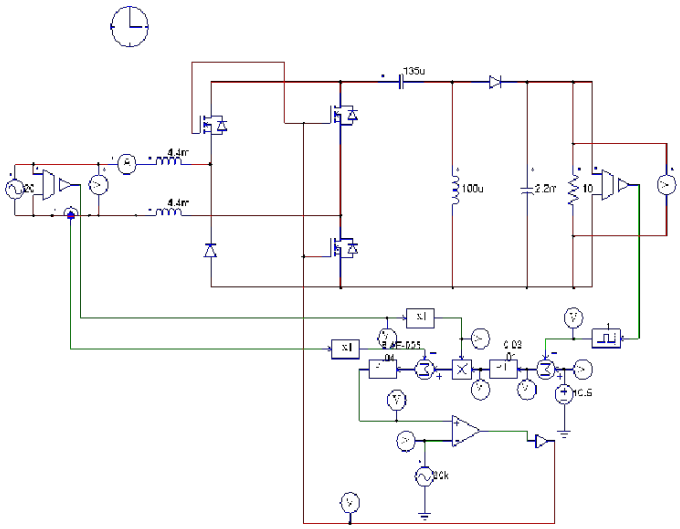


Fig.5. Proposed circuit SEPIC PFC

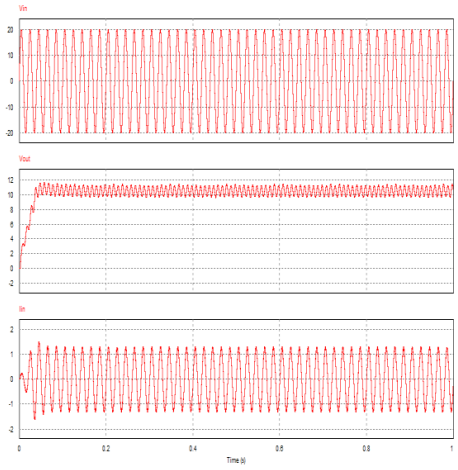

Fig.6. Output Waveforms of Proposed SEPIC PFC

The above output waveforms generated for the switches with the duty cycle of 0.34 and switching frequency of 30KHz for the bridgeless SEPIC PFC converter.

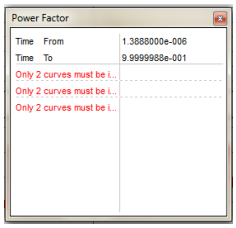


Fig.7. power factor Proposed SEPIC PFC

This above fig 7 represents the power factor. The PF of proposed SEPIC PFC is 99.9%.

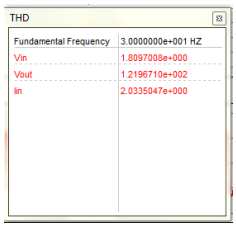


Fig.8. Output Waveforms of Proposed SEPIC PFC

This above fig 8.represents the total harmonic distortion obtained using input current waveform. The THD of proposed SEPIC PFC is 2.033%.

In the fig 6, the output voltage of 10V is generated for proposed bridgeless SEPIC PFC converter with a 120 Hz low frequency ripple. The proposed SEPIC converter is able to reduce the THD 2.03% from 8.93% and improve the power factor to 0.998. The proposed topology provides much better THD and PF compared to conventional one.

IV.CONCLUSION In this paper, a new single phase bridgeless SEPIC PFC converter topology is proposed, analyzed and verified with the simulation results. In order to improve the power factor as well as the THD of the utility grid, the full bridge diode in input is removed. Through simulation the performance of the proposed SEPIC converter topology are compared with the conventional SEPIC converter topology. The proposed converter is able to reduce the THD 2.033% from 8.93% and improve the power factor to 0.998. It is found that the proposed bridgeless SEPIC PFC converter topology provides much better performance than conventional SEPIC PFC converter. The topology is implemented on a converter operating from 20 V AC input to generate 10V DC. The proposed converter topology is proved to be very good option for single phase bridgeless SEPIC PFC solution for lower power equipments especially those requiring high quality input power.

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