International Journal of Pure and Applied Mathematics
Volume 118 No. 24 2018
ISSN: 1314-3395 (on-line version)
url: http://www.acadpubl.eu/hub/
Special Issue

http://www.acadpubl.eu/hub/

A New, Improved ZCS ZVS DC-DC Converter with Nine Level Inverter

K Surendhira Babu, Varun M,
Anirudh V, Shreyas N S
Dept. of Electrical and Electronics Engineering
SRM Institute of Science and Technology, Ramapuram
Chennai, India

May 9, 2018

Abstract

This paper proposes a new, improved zero-current switched (ZCS) and zero-voltage switched (ZVS) DC/DC converter with a standard nine level inverter. The proposed converter achieves ZCS turn-on by implementing coupled-inductors, for their leakage inductance, as well as ZVS turn-off, by employing a snubber capacitor and diode. Minimal losses through conduction are ensured through the inclusion of a voltage multiplier and coupled inductors. Continuous conduction method (CCM) is employed, for a duty cycle greater than 0.5, which ensures that the switching range is not load dependent. The two phase converter is built entirely without the use of auxiliary switches. A high voltage gain and a simple structure make this converter novel for renewable energy applications. The nine level inverter used ensures lower total harmonic distortion, and has an inherent self-voltage balancing ability. The converter/inverter is built to work with a 12V DC input, such as a simple solar panel, and produce a 320V AC output.

***Key Words*:**Zero Voltage Switching (ZVS); Zero Current Switching (ZCS); DC/DC Converter; Multilevel Inverter

1 INTRODUCTION

THE rural parts of India are still very much underdeveloped, in terms of availability of adequate energy for peoples every day needs. Solar power is gaining increasing prominence in the renewable energy scenario, as it is the most abundantly available energy resource. In this paper, a 12V DC source has been chosen as the input, to represent a 12V standard solar panel.

The work in the field of DC-DC converters with high static gain, has very much been progressive in the recent years. Multiple topologies have been presented to achieve higher efficiency, by maintaining low switch voltage and minimal conduction losses. Much work has also been done in the field of zero current switching and zero voltage switching [3, 13]. The development of multiple input zero-current switching converters have proven to be efficient, but with several disadvantages, such as the production of harmonics, and electromagnetic interference in the circuits. There is also considerable switch-off losses, in the case of ZCS turn-on circuits, and switch-on losses in ZVS turn-off circuits. Several other techniques to improve the gain of the converters, such as

switched capacitor [9, 14], switched inductor [9], coupled inductor techniques [2, 5-7, 16, 19], as well as soft commutation techniques [8], have been proposed. In [1, 3, 15, 18], the feasibility of utilizing a boost converter is also discussed. Voltage multipliers are presented in [17, 19, 20]. Clamping circuits for preventing reverse current overvoltages have been discussed in [4, 13, 16]. For smaller applications, multiple input topologies also prove to be less productive, as utilizing a single source instead of many, to obtain the same, if not even better output, would seem as a better idea. Multilevel inverter topologies suitable for the particular application have been discussed in [10-12].

Hence, in this paper, the DC-DC converter proposed, utilizes both ZCS turn-on and ZVS turn-off, to minimize switching losses. The converter also integrates a boost converter and voltage multiplier, along with a coupled inductor. The usage of ZVS eliminates the disadvantages of ZCS, and the nine level inverter used in this paper has voltage boosting capabilities, as well as THD mitigation abilities. Hence, the proposed converter/inverter shown in Fig. 1, provides a solid replacement for multiple input converters, as well

as sole ZCS or ZVS converters.

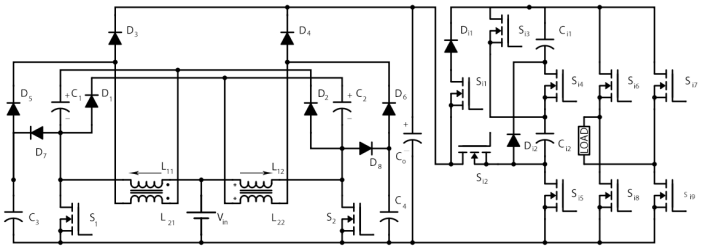

Fig. 1. ZCS ZVS DC-DC Converter with Nine Level Inverter.

2 CONVERTER STRUCTURE AND OPERATION

The proposed two-phase converter circuit consists of switches$S_1 - S_2$, and coupled inductors with primary windings L11 and L12, secondary windings L21 and L22, and output diodes D_3 and D_4, as well as the output filter capacitor Co. The converters base is a conventional boost converter with voltage multiplier circuit, which comprises of the diodes D1 and D2, as well as the capacitors C_1 and C_2. The purpose of including the voltage multiplier circuit, is to boost the static gain to almost twice of that of the conventional boost converter. It also ensures that the switch voltage is brought down to half of the voltage output.

The addition coupled inductors is done to also help improve the static gain, while bypassing drawbacks such as electromagnetic interference. D_3 and $D_4$are placed in series with L_{21} and L_{22}, to also increase the static gain. The ratio of windings turns helps maintain a low switch voltage, while increasing the static gain. The voltage multiplier circuit also acts as a non-dissipative snubber for the switches S1 and S2. The multiplier capacitorsC_1 and C_2 receive the energy stored in the leakage inductance of the coupling inductors. During operation, the output diodes reverse recovery currents energy will get stored in the leakage inductance referred to the secondary side, in $L_{21}$and L_{22}, resulting in an overvoltage atD_3 and D_4, which can be mitigated with the help of the clamping diodes, D_5 and D_6. The clamping diodes ensure the transfer of this leakage inductance energy to the multiplier capacitors. This way, the

undesirable effects of the leakage inductance is removed.

The most efficient coupled inductor polarity is utilized for the converter, as shown in Fig. 2, as it shows the highest static gain and the most optimal operation characteristics. The non-dissipative snubber and the leakage inductances ensure ZCS turn-on, with the leakage inductances creating a limited di/dt.

Including another set of snubber capacitors and diodes, C_3, C_4, D_7 and D_8, ensures the ZVS switch turn-off. dv/dt is limited by the snubber capacitors, with the energy stored in them transferred to the multiplier capacitors, through the secondary windings, clamping diodes, switches.

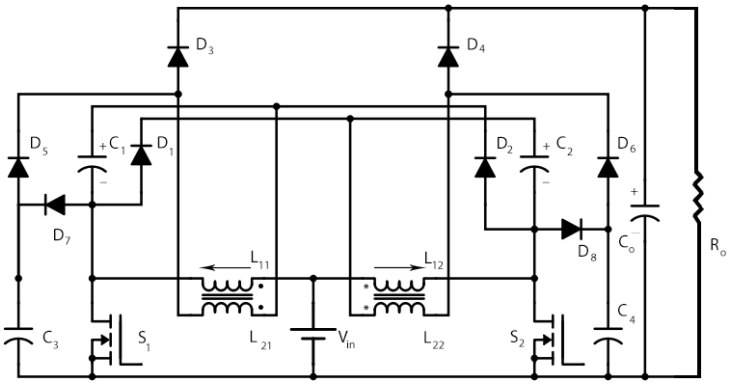

Fig. 2. ZCS ZVS DC-DC Converter.

A. Operating Modes

For the analysis of the converter, the continuous conduction mode (CCM) operation, with switches overlapping, at the duty cycle>0.5, is considered. The leakage inductances of the coupled inductors, output capacitor and voltage multiplier capacitors are all considered in the analysis, with the latter two being considered as a voltage source, in the analysis. The operation of the converter is completely symmetric. Hence, only the first phases operation is defined and presented, with the operation of ZCS switch turn-on and ZVS switch turn-off being discussed in six stages. The waveforms of converter operation can be split into six time intervals, from $t_0 tot_5$.

Stage 1: Before t0, both switches S_1 and S_2 are on and conducting. The input voltage is across both the primary windings of

the inductors, $L_{11} and L_{12}$. Like the conventional boost converter, the aforementioned windings store energy, while none of the diodes in the converter conduct. The inductor current is seen to increase linearly. Stage 1 completes, when S_2 attains turn-off at the instant t_0. This stage is shown in Fig. 3.

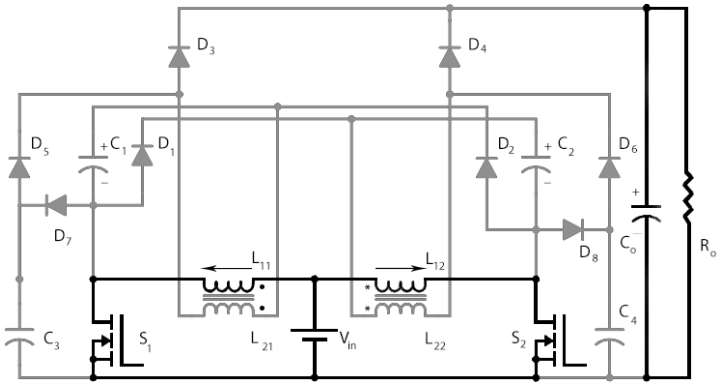

Fig. 3. Stage 1

The inductor voltage and current are shown by (1) and (2).

$$V_{in} = V_{L_{11}} = V_{L_{12}} \tag{1}$$

$$i_{L_{12}} = i_{L_{12}}(t_0) + \frac{V_{L_{12}}}{L_r}.t \tag{2}$$

Stage 2: Immediately at t_0, S_2attains turn-off, with the voltage across C_4 as zero, thereby enabling ZVS turn-off for S_2, with conduction of D_8. The current inL_{12}charges C_4 linearly. The stage finishes when the voltage across C_4equals the voltage acrossC_1, at time instant t_1. This is shown in Fig. 4.

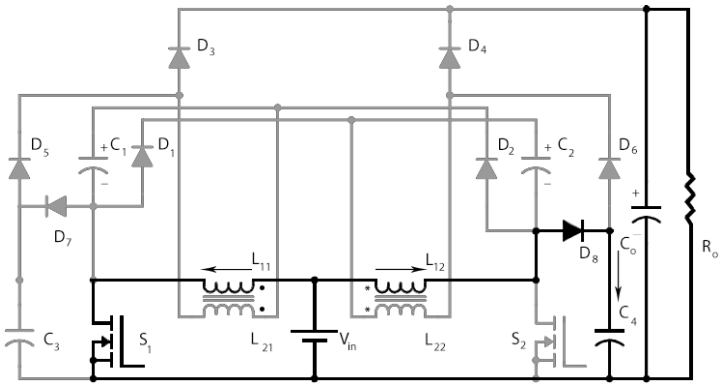

Fig. 4. Stage 2.

The windings turn ratio n is given by (3).

$$n = \frac{N_L secondary}{N_L primary} \tag{3}$$

The maximum value of the switch voltage is:

$$V_{S1} = V_{S2} = V_{in}.\frac{1}{1-D} \tag{4}$$

Voltage in the primary winding L_{12} is:

$$V_{L_{12}} = V_{C1} - V_{in} = V_{in}.\frac{1}{1-D} - V_{in} \tag{5}$$

Voltage in the secondary winding L_{22} is:

$$V_{L_{22}} = V_{L_{12}}.n = (V_{in}.\frac{1}{1-D} - V_{in}).\frac{N_{L_{22}}}{N_{L_{12}}} \tag{6}$$

Stage 3: At the instant t_1, D_2 and S_1 start transferring the energy in inductor$L_{12}, toC_1.D_8$does not conduct, and output energy is transferred from $L_{12}toD_4$, through L_{22}. The current atD_2 gradually reduces to zero, at the time t_2. This is shown in

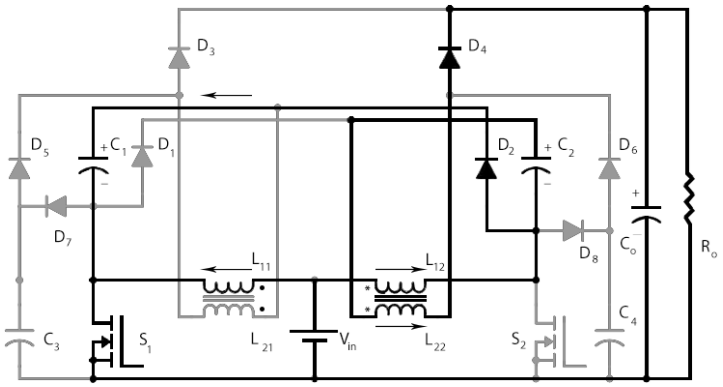

Fig. 5. Stage 3.

Stage 4: At the time instantt_2, C_1 charges fully, and D_2 stops conducting. At this time period, D_4continues to supply energy to the output, until the time period t_3, at which time the switchS_2 will switch on, as shown in Fig. 6.

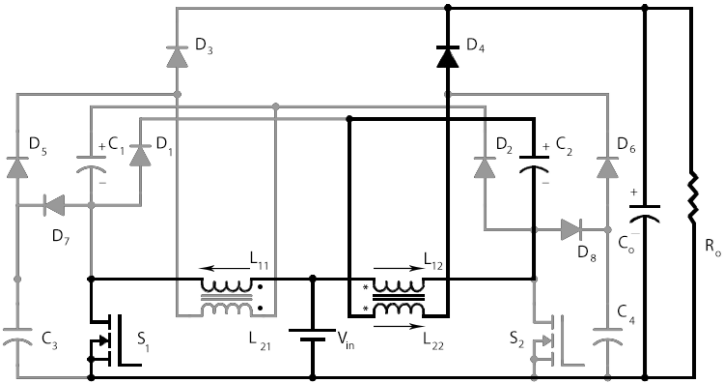

Fig. 6. Stage 4.

Stage 5: At t_3, S_2 switches on, with ZCS. The di/dt value is limited by the leakage inductance, thereby ensuring that the current value at turn-on is zero. Reverse recovery problems are also mitigated with the help off the *di/dt* limiting by the leakage inductance. The current across D_4 decreases gradually and linearly, with minimal *di/dt*, until it reaches zero, at t_4, where D_4 stops conducting, as illustrated in Fig. 7.

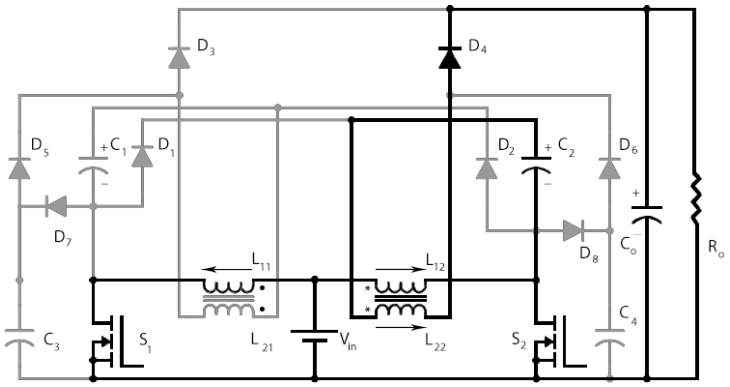

Fig. 7. Stage 5

Stage 6: At the instant t_4, when D_4 stops conducting, the leakage inductance referred to the secondary side starts storing the reverse recovery current. At this instant, D_6, the clamping diode, immediately starts operating as a freewheeling diode, ensuring the transfer of energy from the leakage inductance to the capacitor C_2. Simultaneously, the stored energy from C_4 is transferred to C_2, through$D_6, S_2 and L_{22}$. This is shown in Fig. 8.

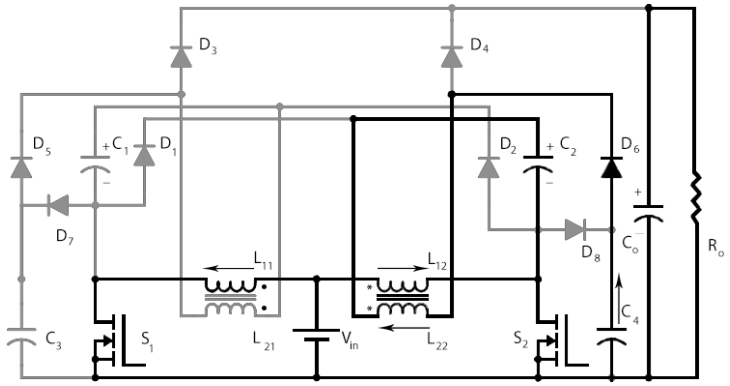

Fig. 8. Stage 6.

Finally, at the end of the first phase, C_4 discharges completely, at the instant t_5, which stops D6 from conducting. This marks the end of the first phase, where the converter returns to the first stage, for the second phase of operation to begin.

The operational waveforms are shown in Fig. 9:

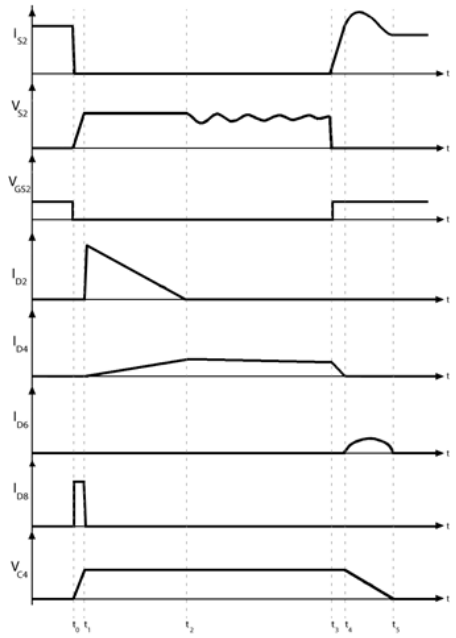

Fig. 9. Operational Waveforms

Snubber capacitor current and voltage can be calculated as:

$$i_{Csnubber}(t) = \sqrt{\frac{C_{eq}}{L_k.n^2}}.n.V_{in}.\cos(\omega_0.t) \tag{7}$$

$$V_{Csnubber}(t) = (n.V_{in}) - (n.V_{in} - V_{in}.\frac{1}{1-D}) \tag{8}$$

C_{eq} and ω_0 are given by:

$$C_{eq} = \frac{C_{multiplier}.C_{snubber}}{C_{multiplier} + C_{snubber}} \tag{9}$$

$$\omega_0 = \frac{1}{\sqrt{L_k.n^2.C_{eq}}} \tag{10}$$

The value of the initial condition of the snubber capacitors is equal to that of (4). The resonant period is given by (11).

$$T_0 = \frac{2\pi}{\omega_0} \tag{11}$$

The output voltage V0, along with the gain, is shown below:

$$V_0 = V_{S2} + V_{C2} + V_{L_{22}} \tag{12}$$

$$V_0 = [(\frac{V_{in}}{1-D}) + (\frac{V_{in}}{1-D}) + (\frac{V_{in}}{1-D} - V_{in}).n] \tag{13}$$

$$\frac{V_0}{V_i} = \frac{2 + D.n}{1-D} \tag{14}$$

The coupling coefficient K can be calculated as follows:

$$K = \frac{L_m}{L_m + L_k} \tag{15}$$

Where L_k is the leakage inductance, and$L_m$is the magnetizing inductance, given by (16).

$$L_{11} = L_{12} = L_m \tag{16}$$

When the static gain of the converter is increased with the turns ratio of the winding n, while maintaining the same switch voltage, and considering a non-ideal condition with the coupling of the inductor, the leakage inductance Lk and magnetizing inductance Lm come into consideration. Hence, K comes into consideration. The static gain (considering a turns ratio of 2) hence becomes:

$$\frac{V_0}{V_i} = \frac{2 + D.n.k^2}{1-D} \tag{17}$$

3 Inverter Structure and Operation

Fig. 10 shows the topology of the nine-level inverter to be used along with the converter proposed above. Table I lists the switching patterns for the nine-level inverter. Compared to other multilevel inverter, the chosen nine-level inverter employs far lesser components, while having more voltage levels. The inverter employs only two capacitors, which simplifies the modulation algorithm, while also ensuring lower Total Harmonic Distortion (THD) and electromagnetic interference, due to the parallel connection of the capacitors. The inverter also has self-voltage balancing abilities, which also simplifies modulation algorithms and driving circuits.

Pulse-Width modulation (PWM) is utilized to control the inverter. Four quasi-square waves are utilized to obtain nine-level modulation. They can be labelled as v1, v2, v3 and v4. The input voltage is Vdc. The amplitudes are $\pm 2V_{dc}, \pm 3V_{dc}/2, \pm V_{dc}, \pm V_{dc}/2$ and $0.\theta_1, \theta_2, \theta_3, \theta_4 and \theta_5$ are the conducting angles, whose values must be set according to the following condition:

$$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 = 90^\circ \tag{18}$$

Each waveforms Fourier analysis is shown below.

$$v_{0j} = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\cdots}^{\infty} \frac{\cos(k\theta_j)}{k} \sin k\omega t \tag{19}$$

where i has the values 1, 2, 3, and 4.

The Fourier analysis of the output voltage is given by:

$$v_0 = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\cdots}^{\infty} \sum_{i=1}^{4} \frac{\cos(k\theta_j)}{k} \sin k\omega t \tag{20}$$

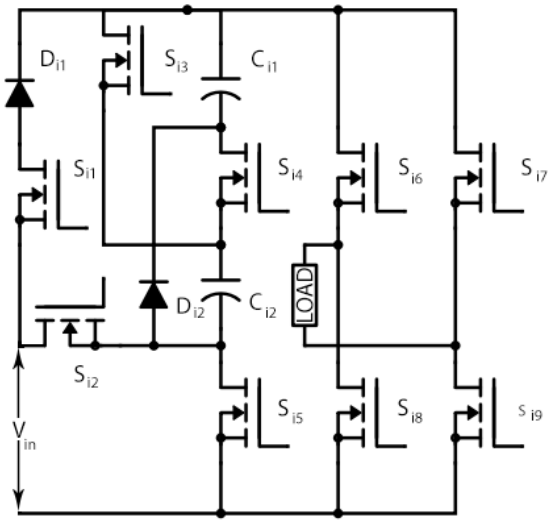

Fig. 10. Nine-Level Inverter Topology.

TABLE I. STATES OF CAPACITORS, SWITCHES AND DIODES

Voltage levels	$2V_{dc}$	$3V_{dc}/2$	V_{dc}	$V_{dc}/2$	0	$-V_{dc}/2$	$-V_{dc}$	$-3V_{dc}/2$	$-2V_{dc}$
C_1	Disch.	Disch.	Char.	Disch.	Nil.	Disch.	Char.	Disch.	Disch.
C_2	Disch.	Disch.	Char.	Disch.	Nil.	Disch.	Char.	Disch.	Disch.
D_1	Rev.	Rev.	Fwd.	Rev.	Rev.	Rev.	Fwd.	Rev.	Rev.
D_2	Rev.	Fwd.	Rev.	Fwd.	Rev.	Fwd.	Rev.	Fwd.	Rev.
S_{11}	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S_{12}	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
S_{13}	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF
S_{14}	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
S_{15}	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF
S_{16}	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
S_{17}	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON
S_{18}	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON
S_{19}	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF

the words Disch. and Char. indicate if the capacitors are discharging or charging, and the words Rev. and Fwd. denote if the diodes are in forward or reverse biased condition. The ON and OFF symbols indicate if the switches are conducting or not.

4 SIMULATION RESULTS

The converter/inverter prototype presented in the paper, is simulated using MATLAB v2017a, with SIMSCAPE components. The simulation was run for an input of 12V DC, and consistently gave an output of 320V AC. The simulated output also shows the nine-level output waveform of the multilevel inverter. Fig. 12 shows the input waveform, and Fig. 13 shows the output waveform of the inverter. The values of the components used are shown in Table II.

TABLE II. COMPONENTS USED IN SIMULATION

Part	Value
D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_{11}, D_{12}	R_{on} = 0.001Ω, V_f = 0.8V, R_s = 500Ω C_s = 250nF
C_1, C_2, C_3, C_4	Capacitance = 120µF
S_1, S_2	R_{on} = 0.1Ω, R_d = 0.01 Ω, V_f = 0V, R_s = 100kΩ, C_s = 8 F, S_1 Pulse Width = 50, Delay = 0 S_2 Pulse Width = 50, Delay = *1/2f*
L_{11}, L_{21}(and L_{12}, L_{22})	R_1 = 1.1Ω, L_1 = 1.1mH, R_2 = 1.1Ω, L_2 = 1.1mH, n = 1:1
V_{in}	12V
C_o	Capacitance = 70µF
S_{11}, S_{12}, S_{13}, S_{14}, S_{15}, S_{16}, S_{17}, S_{18}, S_{19}	R_{on} = 0.1Ω, R_d = 0.01 Ω, V_f = 0V, R_s = 100kΩ, C_s = 8 F
C_{11}, C_{12}	Capacitance = 1000µF

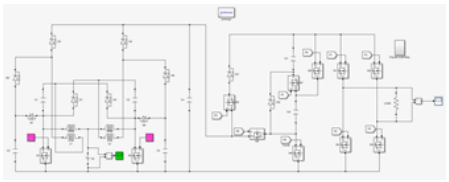

Fig. 11: Simulation Diagram of the Converter/Inverter.

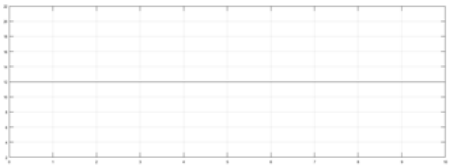

Fig. 12: Input Voltage Waveform.

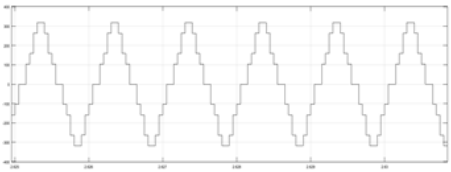

Fig. 13: Output Voltage Waveform.

5 CONCLUSION

In this paper, a ZCS ZVS DC/DC converter with a nine level inverter is proposed. The operation of the converter and inverter, along with the specifications and simulation results are shown and discussed. The usage of ZVS along with ZCS helps overcome the disadvantages of ZCS, such as the generation of electromagnetic interference, and the production of harmonics. The inverter also helps reduce the THD by utilizing nine levels, while also ensuring fewer components, thereby ensuring lower costs, while maintaining high efficiency. Ultimately, the disadvantages of ZCS are overcome with the help of implementing ZVS and the nine-level inverter, while ensuring minimal switching losses.

References

[1] F. L. Tofoli, D. C. Pereira, W. J. Paula, D.S. O. Jnior, "Survey on Non-Isolated High-Voltage Step-Up DCDC Topologies Based on the Boost Converter", IET Power Electron., vol. 8, no.10, pp. 2044-2057, 2016.

[2] Y. Ye, K.W. E. Cheng and S. Chen, "High Step-Up PWM DC-DC Converter with Coupled-Inductor and Resonant Switched-Capacitor", IEEE Trans. on Power Electron., Nov. 2016.

[3] S. Sathyan , H. M. Suryawanshi , B. Singh , C. Chakraborty , V. Verma and M. S. Ballal, "ZVSZCS High Voltage Gain Integrated Boost Converter for DC Microgrid", IEEE Trans. on Ind. Electron., vol. 63, no. 11, pp. 6898-6908, Nov. 2016.

[4] C. M. C. Duarte and I. Barbi, "A Family of ZVS-PWM Active-Clamping DC-to-DC Converters: Synthesis, Analysis, Design, And Experimentation," IEEE Trans. Circuits Syst. I, Fundam Theory Appl., vol. 44, no. 8, pp. 698-704, Aug. 1997.

[5] G. L-S. Yang, T-J. Liang and J-F. Chen, "Transformerless DCDC Converters With High Step-Up Voltage", IEEE Trans. on Ind. Electron., vol. 56, no. 8, pp. 3144- 3152, Aug. 2009.

[6] Q. Zhao and F. C. Lee, High-efficiency, High Step-Up DCDC Converters", IEEE Trans. on Power Electron, vol. 18, no. 1, pp. 65-73, Jan. 2003.

[7] H-L. Do, "A Soft-Switching DC/DC Converter With High Voltage Gain", IEEE Trans. on Power Electron., vol. 25, no. 5, pp. 1193-1200, May 2010.

[8] S. Park and S. Choi, " Soft-Switched CCM Boost Converters With High Voltage Gain for High-Power Applications", IEEE Trans. on Power Electron., vol. 25, no. 5, pp. 1211- 1217, May 2010.

[9] B. Axelrod, Y. Berkovich and A. Ioinovici, Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DCDC PWM Converters, IEEE Trans. on

Circuits and Systems - I: Regular Papers, vol. 55, no. 2, pp. 687-696, Mar. 2008.

[10] G. Buticcchi, E. Lorenzani and G. Franceschini, A Five-Level Single-Phase Grid-Connected Converter for Renewable Distributed Systems, IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 906-918, Mar. 2013.

[11] J. Liu, J. Wu, J. Zeng, H. Guo, A Novel Nine-Level Inverter Employing One Voltage Source and Reduced Components as High Frequency AC Power Source, IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2939-2947, April 2017.

[12] G. Buticchi, D. Barater, E. Lorenzani, C. Concari and G. Franceschini, A Nine-Level Grid-Connected Converter Topology for Single-Phase Transformerless PV Systems, IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3951- 3960, Aug. 2014.

[13] W. Li, W. Li, Y. Deng, and X. He, "Single-Stage Single-Phase High-Step-Up ZVT Boost Converter For Fuel-Cell Microgrid System," IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3057-3065, Dec. 2010.

[14] A. A. Fardoun and E. H. Ismail, "Ultra Step-Up DC- DC Converter with Reduced Switch", in IEEE International Conference on Sustainable Energy Technologies, 2008.

[15] G. Henn, R. Silva, P. Praa, L. Barreto D. Oliveira, Interleaved Boost Converter with High Voltage Gain, IEEE Trans. on Power Electron., vol. 25, no. 11, pp. 27532761, Nov. 2010.

[16] W. Li and X. He, An Interleaved Winding-Coupled Boost Converter With Passive Lossless Clamp Circuits, IEEE Trans. on Power Electron., vol. 22, no. 4, pp. 1499-1507, Jul. 2007.

[17] W. Li, Y. Zhao, Y. Deng and X. He, "Interleaved Converter With Voltage Multiplier Cell for High Step-Up and High-Efficiency Conversion", IEEE Trans. on Power Electron., vol. 25, no. 9, pp. 2397 - 2408, Apr. 2010.

[18] C. W. Li and X. He, Review of Non-Isolated High Step- Up DC/DC Converters in Photovoltaic Grid-Connected Applications, IEEE Trans on Ind. Electron, vol. 58, no. 4, pp. 1239-1250, Apr. 2011.

[19] H. Liu, F. Li, and J. Ai," A Novel High Step-Up Dual Switches Converter With Coupled Inductor and Voltage Multiplier Cell for a Renewable Energy System", IEEE Trans. on Power Electron., vol. 31, no. 7, pp. 4974-4983, Jul. 2016.

[20] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli and R. Gules, Voltage Multiplier Cells Applied to Non-Isolated DCDC Converters, IEEE Trans. On Power Electron., vol. 23, no 2, pp. 871-887, Mar. 2008.