Design And Analysis Of Diode Clamped Multilevel Inverter With Reduced Number Of Switches Using Multicarrier Spwm

MD Imran Hussain¹, Mohankumar.J², Dr.E.Sheeba Percis³, Dr.A.Nalini⁴,
¹Department of EEE, ²Post Graduate, ³,⁴ Associate Professor, Dr. MGR E & RI, Chennai.
VIT University, Vellore.

May 3, 2018

Abstract

In this paper the design and analysis of the diode clamped inverter with reduced number of switches is discussed. The diode clamped inverter for seven levels is designed and implemented. The voltage balancing is done with the help of resonant series switched capacitor (RSSC) converter. Multicarrier Sinusoidal Pulse width modulation (SPWM) is employed for generating firing pulses to the switches in the inverter. The performance of the proposed circuit is compared with the existing cascaded multilevel inverter. The comparison is made with respect to the current and voltage THD, variation in modulation index and carrier frequency. The Voltage-THD and Current-THD are calculated at various modulation indices and carrier frequencies. The simulation is done in MATLAB/SIMULINK. The hardware implementation is also carried out using DSPACE.RTS1202 software tool is used for interfacing in Dspace.

Key Words: Multilevel inverters, Pulse width modulation techniques, seven level inverter, Multi carrier sinusoidal
1 INTRODUCTION

Due to the development in the field of science and technology the demand and the quality of electric power is increased. Various power conversion techniques are promoted using power semiconductor switches. One of the popular circuits used for power conversions inverter which is used for converting DC to AC. The concept of multilevel inverters involves addition of different voltage levels to create a stepped waveform which is smoother. The advantage of using multilevel inverter is it has low voltage stress and lower dv/dt and reduction in harmonics. The disadvantage is, with the increase in number of voltage levels the design for the inverter becomes complicated and number of components required is more. At present situation in power systems the harmonic pollution is increasing. According to IEEEstd. 1547 and UL 1741, harmonics should be specified within the limits.

From industry point of view multilevel inverters are used for high power applications. With regards to high power applications the choice in the selection of the switch is essential. Though IGBTs are used for high power applications it has high conduction losses. So MOSFETs are used for high voltage applications.

Recently researchers are focusing to use this inverter for low power applications by developing suitable optimization algorithms [3], in order to enhance the total harmonic distortion (THD). Multilevel inverters requires large number of drivers circuits and switches because as the level increases harmonic content decreases but the cost of component increases. The commercially available multilevel inverters are Diode clamped multilevel inverter, flying capacitor (FC), Cascaded H bridge multilevel inverter. Diode clamped inverters does not possess any voltage balancing issues when used below three levels. When the voltage level is above 4 there is a problem in voltage balancing. There is various voltage balancing techniques.
2 CIRCUIT TOPOLOGY

The above figure represents a Diode clamped multilevel inverter with reduced number of switches. An input voltage divider is composed of three series capacitors $C_1, C_2,$ and $C_3$. The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is sent to output terminal by H-bridge which is formed by four MOSFET. The seven levels in the output voltage are as follows: $(+1/3V_{dc}, +2/3V_{dc}, V_{dc}, -1/3V_{dc}, -2/3V_{dc}, -V_{dc})$.

**Mode 1:**

During the positive half cycle of the output voltage, in order to produce output voltage of $1/3V_{dc}$ the switch $S_1$ is turned on. The capacitor $C_1$ is charged and the voltage across the H-bridge is $1/3V_{dc}$. The switches $S_5$ and $S_8$ are turned on. The above figure shows the current path.

**Mode 2:**
In order produce the output voltage $2/3V_{dc}$ the switches $S_1$ and $S_4$ are turned on. The energy is provided by the capacitors $C_1$ and $C_2$. The switches $S_5$ and $S_8$ are turned on. The output voltage across the H-bridge is $2/3V_{dc}$. The direction of the output current is shown in the figure.

**Mode 3:**
In order to produce the output voltage $V_{dc}$ the switches $S_1$ and $S_2$ are turned on. The capacitors $C_1, C_2, C_3$ are charged. The switches $S_5$ and $S_8$ are conducting to produce output voltage $V_{dc}$ across the cascaded H-bridge.

**Mode 4:**

In order produce the output voltage $-V_{dc}/3$ the switches $S_3$ and $S_6$ are turned on. The capacitors $C_4, C_5, C_6$ are charged. The switches $S_7$ and $S_9$ are conducting to produce output voltage $-V_{dc}/3$ across the cascaded H-bridge.
During negative half cycle, in order to produce output voltage -1/3Vdc, the switch $S_2$ is turned on. The energy is provided by the capacitor $C_3$. The switches $S_6$ and $S_7$ are conducting. The voltage across the cascaded H-bridge is -1/3Vdc.

**Mode 5:**

![Figure 6 Output voltage of -2Vdc](image)

In order to produce the output voltage -2/3Vdc, the switches $S_2$ and $S_3$ are turned on. The capacitors $C_2$, $C_3$ are charging. In H-bridge the switches $S_6$ and $S_7$ are conducting and the voltage across the H-bridge is -2/3 Vdc.

**Mode 6:**

![Figure 7 Output voltage of -Vdc](image)

**Mode 7:**

![Figure 8 Output voltage of Zero](image)

In order to produce output voltage 0, the switches $S_5$, $S_7$ are conducting. The output voltage across the load terminals is zero.

**RESONANT SERIES CAPACITOR CONVERTER (RSCC)**
The voltage balance across the capacitors cannot be maintained in the diode clamped inverters with more than 4 levels. Because the charge flowing through the capacitors is not same in each half cycle. So there is a need of an additional voltage balancing circuit. Resonant series switched capacitor converters is used for voltage balancing. The resonant frequency is determined from the above waveforms by $L_r$ and $C_r$. When two switches denoted by $S$ are in on state ($V_{c1}, V_{c2}$) and $C_r$ is charged by $C_1$. When two switches denoted by $S_p$ are in on state $C_2$ is charged by $C_r$. Thus the voltage across the capacitors are balanced by following the above switching operation. By changing the amplitude of $i_r$ the voltage across the $V_{c1}$ and $V_{c2}$ are balanced without any feedback control. The RSCC is operated at zero current switching, so the switching loss across the switch cannot be a problem.

3 CONTROL SCHEME

The modulation technique used is multicarrier sinusoidal pulse width modulation. In this technique, in MSPWM, the technique used is phase disposition (PD) technique. There are three kinds of SPWM techniques like phase disposition (PD), phase opposition disposition (POD), Advanced phase opposition disposition (APOD) technique. In multicarrier SPWM technique triangular waves are taken as a carrier wave and is compared with that of the sinusoidal wave, which is taken as a reference wave. The pulses are produced and are given to that of the respective switches of the inverter circuit. The frequency of the carrier wave determines the switching frequency of the inverter. The number of carrier waves taken depends upon the...
number of switches. If all the carrier waves are taken in the same phase, it is called phase disposition (PD) technique. The advantage of using PD technique is, it is less complicated to realize and the THD produced by this method is very less. The Phase Opposition Disposition (POD) method, having the carriers above the zero line of reference voltage and is in out of phase by 180 degrees. In APOD technique each carrier wave is shifted 180 degrees from its adjacent one. The modulation index $m_a$ is determined by calculating the peak value of the reference wave to that of the peak value of the carrier wave.

$$M_a = \left(\frac{V_{sin}}{3V_{tri}}\right) \quad V_o = m_a V_{dc}$$

The above figure shows the simulation circuit of cascaded multicell inverter. It consists of switches and an auxiliary switch with four
diodes and two voltage sources. The pulse width modulation technique used is multicarrier pulse width modulation. The proposed circuit is compared with that of cascaded multicell-inverter circuit.

![Simulation circuit of the diode clamped inverter when connected to Induction motor load](image1)

**Figure 10** Simulation circuit of the diode clamped inverter when connected to Induction motor load

**Hardware layout**

![Hardware implementation of the Cascaded MLI](image2)

**Figure 11** Hardware implementation of the Cascaded MLI

DC source: Generally in this thesis we described about renewable energy source. But due to the unavailability of solar panel as an input to the converter. We have taken programmable D.C supply as one supply source and the other two supply sources from the RPS Cascaded multilevel H-Bridge inverter. The layout of the circuit is done in ilium sheet. MOSFETs numbered as IRF840 are used as switches for this inverter. As they can withstand voltage rating of 500V, 8A. And the power diodes numbered as MUR1560 are used.

Driver circuit: The driver circuit used is opto-isolator TLP250, which is used for providing the isolation from the board to the Dspace. The transformer (15-0-15)v is connected to the driver board. The output of the driver board is connected with the help of male to female connectors to the Dspace 16 bit pin. The pulses are observed in the DSO.

Dspace: The pulses for the switches are developed using dspace.
4 RESULTS AND DISCUSSION

Figure 12 Output voltage and current waveforms of the seven level proposed inverter circuit.

The output voltage and current waveform of the proposed diode clamped inverter circuit is shown below. It consists of seven levels in the output voltage.

Figure 13 Speed characteristics of the motor

The THD analysis without filter for the proposed circuit is shown below and it was around 18.19%. The THD is further reduced by connecting a filter at output side

Figure 14 THD analysis without filter

Figure 15 THD analysis with filter
The THD can be further reduced by connecting a filter at the output side. The THD analysis when connected to an L C filter at the output side is around 7.42%. The L and C values are calculated from the formulas. The filter circuit chosen is low pass LC filter. The values of L and C can be determined by

$$F_r = 1/(2 \pi \sqrt{LC})$$

The switching frequency of the carrier wave is 1 KHz and the value of C is assumed to be around 10 Micro-farad and the value of L is determined. Based on the tuning of L and C values in the output side the THD can be reduced.

Figure 16 Output voltage and current waveform of Cascaded multicell inverter

The reference wave is taken as Sine wave and its frequency is around 50Hz. The technique that is used in MSPWM is PD technique. In this technique all the carrier waves are in phase with each other. This technique when used for the inverter gives less THD in the output voltage. The output voltage and current waveforms of Cascaded multicell inverter is shown below. The switching frequency of the carrier wave is taken as 1Khz and that of the reference wave is taken as 50Hz.

Figure 17 THD analysis of Cascaded multicell inverter

Hardware output wave-form
5 Conclusion

The design and analysis of a diode clamped inverter with reduced number of switches is carried out. The voltage THD and current THD at varying modulation indices and carrier frequency is calculated. It was observed that the proposed multilevel inverter is giving less THD when compared to that of cascaded multicell inverter. The voltage balancing of the input capacitors in a diode clamped inverters is done by using resonant series switched capacitor converter. The voltage stress and switching losses are less for the proposed inverter. The PD technique used is Multicarrier SPWM technique. The PD technique gives better reduction in THD. The above inverter is used for drive applications.

References


photovoltaic system.” IEEE transactions on industrial electronics 58, no. 6 (2011): 2435-2443.


