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Fast FIR Algorithm based symmetric FIR filter using Han-Carlson adder and vedic multiplier

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Abstract

Efficient FIR filter is the need of various digital signal processing applications. In this paper, fast FIR algorithm based parallel symmetric FIR filter using Han-Carlson adder and vedic multiplier is proposed. FFA algorithm used in the architecture reduces the multiplier count as compare to the traditional parallel design. In order to improve the performance of the proposed filter design, recently developed vedic multiplier based on BEC unit and Han-Carlson adder is used. Proposed design for two and three parallel FIR filter of order 24 and 72 are implemented using VHDL in Xilinx 14.2 navigator. The implementation results of the proposed architecture shows that it provides the better speed performance and low area requirement as compared to the conventional one. Due to higher speed and low hardware, proposed

architecture is useful in many signal processing and modern communication system.

***Key Words*:**Fast FIR algorithm (FFA), Urdhva-Tiryakabhyam sutra, FPGA, DSP

1 Introduction:

Digital filters are considered to be the main fundamental block in almost every DSP applications. Over the past several decades various architecture of digital filter has been implemented either on hardware or in software [1]. Due to speedy and reliable process hardware implementation approach is preferred for filter design [2]. With the advantage of phase linearity and stability FIR is preferred in many DSP applications like defence equipments, telecommunication, audio and video processing system, etc [3]. These applications required large order FIR filter to get better cut offs and roll of characteristics. This increases number of arithmetic computations, power dissipation and resulted in more bulky system [4].

To make efficient FIR filter and improve the throughput of the system, many pipelined [5, 6] and parallel architecture [7-10] has been proposed. Pipeline architecture reduces the critical path delay using the different datapath latches. But with the number of increasing latches, the system latency also increases. On the other hand, parallel processing is used in multiple input multiple output (MIMO) DSP applications to enhance the latency of architecture. L-parallel filter design increases the speed of the architecture but it replicates the hardware L times.

To reduce the hardware cost of parallel FIR filter, fast FIR algorithm (FFA) [8] has been proposed which reduces one fourth hardware over the traditional one. Further with few modifications, FFA algorithm has been saved some more hardware for the symmetric FIR filter using the inherent property of symmetric coefficients [10]. But the FFA based parallel architectures have been presented with the conventional multiplier and adders only. The multiplier and adder play the vital role in the performance of the FIR filter. Several architectures have been developed for the multiplier and adder. The comparative study [11] shows that among different architectures, Han-Carlson adder consumes minimum area and vedic multiplier provides good result in terms of delay. In this paper,

FFA based symmetric FIR filter design is explored with the recently developed vedic multiplier [12] and Han-Carlson adder [13]. Urdhva-Tiryakbhyam sutra based vedic multiplier using BEC unit and Han-Carlson adder used in the proposed design provides the advantage of higher speed and lesser area requirement over the conventional one.

The rest of the paper has been organised as follows. Section II describes the fast FIR algorithm (FFA). Section III describes the proposed structure for symmetric FIR filter and its importance. Section IV explains the synthesis and simulation results of proposed FIR architecture. Section V describes the performance analysis details of proposed FIR filter.

2 Fast FIR algorithm

Digital FIR filters are typically used to modify or alter the attributes of a signal in the time or frequency domain [2]. If p(n) is the input signal, h(n) is the impulse response of the filter with the order N and q(n) is the output of the signal then the general FIR filter equation [3] is,

$$q(n) = \sum_{i=0}^{N-1} h(i)p(n-i) \tag{1}$$

The fast FIR algorithm (FFA) for symmetric FIR filter is described as follows:

A. 2 ×2 FFA (L = 2)

The (2-by-2) FFA results in a 2-parallel filtering structure. The traditional 2-parallel filtering structure has [8],

$$\begin{aligned} Q_0 + z^{-1}Q_1 &= (H_0 + z^{-1}H_1)(P_0 + z^{-1}P_1) \\ &= H_0P_0 + z^{-1}(H_0P_1 + H_1P_0) + z^{-2}H_1P_1 \end{aligned} \tag{2}$$

which implies that

$$\begin{aligned} Q_0 &= H_0P_0 + Z^{-2}H_1P_1 \\ Q_1 &= H_0P_1 + H_1P_0 \end{aligned} \tag{3}$$

The parallel structure shown by equation (3) requires four N/2 length subfilter block, 2N multipliers and 2(N - 1) adder. In order to reduce the hardware, the same two-parallel filtering structure described above can be written for symmetric FIR filter in FFA form [10] as

$$Q_0 = \{\frac{1}{2}[(H_0 + H_1)(P_0 + P_1) + (H_0H_1)(P_0P_1)]H_1P_1\} + z^{-2}H_1P_1$$

$$Q_1 = \frac{1}{2}[(H_0 + H_1)(P_0 + P_1) + (H_0H_1)(P_0P_1)] \tag{4}$$

The implementation of (4) based on FFA algorithm is shown in fig. 1. It requires only two N/4-length and one N/2-length subfilter block, N multipliers, (N-3) subfilter adders and 4 post-processing adders. So clearly it saves 50% hardware over the traditional parallel filter.

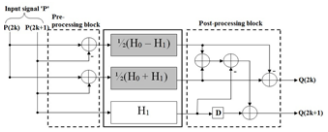

Fig. 1: 2-parallel symmetric FIR filter implementation using FFA

B. 3 × 3 FFA (L = 3).

The (3-by-3) FFA produces a parallel filtering structure of block size 3. A traditional three-parallel FIR filter can be expressed as [8].

$$Q = Q_0+z^{-1}Q_1+z^{-2}Q_2 = (P_0+z^{-1}P_1+z^{-2}P_2)(H_0+z^{-1}H_1+z^{-2}H_2)$$

$$= P_0H_0 + z^{-1}(P_0H_1 + P_1H_0) + z^{-2}(P_0H_2 + P_2H_0 + P_1H_1)$$

$$+z^{-3}(P_1H_2 + P_2H_1) + z^{-4}P_2H_2$$

which implies that

$$Q_0 = H_0P_0 + z^{-3}(H_1P_2 + H_2P_1)$$

$$Q_1 = (H_0P_1 + H_1P_0) + z^{-3}H_2P_2$$

$$Q_2 = H_0P_2 + H_1P_1 + H_2P_0 \tag{5}$$

Same as 2-by-2, the equation (5) can also be computed for the symmetric FIR filter based on FFA [10] as,

$$Q_0 = \frac{1}{2}[(H_0 + H_1)(P_0 + P_1) + (H_0H_1)(P_0P_1)]H_1P_1 + z^{-3}$$

$$\{(H_0+H_1+H_2)(P_0+P_1+P_2)-(H_0+H_2)(P_0+P_2)\frac{1}{2}[(H_0+H_1)(P_0+P_1)-(H_0H_1)(P_0P_1)]H_1P_1\}$$

$$Q_1 = \frac{1}{2}[(H_0 + H_1)(P_0 + P_1) - (H_0H_1)(P_0P_1)] + z^{-3}$$

$$\{\frac{1}{2}[(H_0+H_2)(P_0+P_2)+(H_0H_2)(P_0P_2)]\frac{1}{2}[(H_0+H_1)(P_0+P_1)+(H_0H_1)(P_0P_1)]+H_1P_1\}$$

$$Q_2 = \frac{1}{2}[(H_0 + H_2)(P_0 + P_2) - (H_0H_2)(P_0P_2)] + H_1P_1 \tag{6}$$

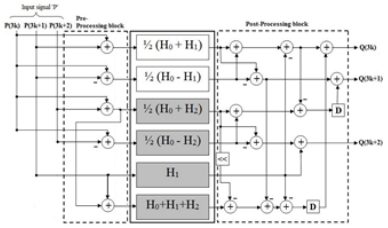

Fig. 2: 3-parallel symmetric FIR filter implementation using FFA

The 3-by-3 parallel symmetric FIR architecture is shown in fig. 2. It consists of four subfilter blocks with symmetric coefficients as highlighted in the diagram. With the increased number of subfilter blocks with symmetric coefficients, it has been saved more multiplier and adders.

For higher level of parallelism like 4, 6, 8, etc., one can cascade the 2-by-2 and 3-by-3 design to get the desired architecture.

3 PROPOSED STRUCTURE FOR SYMMETRIC FIR FILTER

In this section proposed architecture of parallel symmetric FIR filter based on FFA algorithm is presented. For this conventional FFA

[10] based symmetric FIR filter structure is explored with the recently developed vedic multiplier [12] and Han-Carlson adder [13]. FFA algorithm is beneficial for digital symmetric FIR filter in terms of the area. The proposed architecture using Urdhva-Tiryakbhyam sutra based vedic multiplier with BEC unit and Han-Carlson adder provides the multiple advantages such as reduced critical path delay and hardware cost over the conventional one. The proposed architecture of L-parallel symmetric FIR filter of order N is shown in fig. 3,

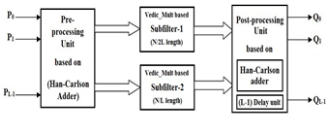

Fig. 3: Proposed architecture for the L - parallel symmetric FIR filter

The pre-processing and post processing unit in proposed design are same as described in the earlier section. But in order to improve performance, it contains Han-Carlson adder instead of carry-save adder. Two kinds of subfilter blocks are defined in the design which contains the coefficient set of the filter according to the FFA algorithm. The subfilter-1 block represents the block with symmetric coefficient set. It is shown in fig. 4 which consists of half the number of vedic multiplier, i.e., (N/2L) for an L-parallel FIR filter of order N.

For a symmetric FIR filter, h(n) = ± h(n-N-1) Consecutively, for e.g., FIR filter with order 24 has, h(0) ±h(1) = ± (h(22)± h(23))· · · · · ·

Hence the output of each multiplier fed to the two adders to compute two taps.With reductions in the hardware cost, it also save half the time consume in the computation of the multiplier.

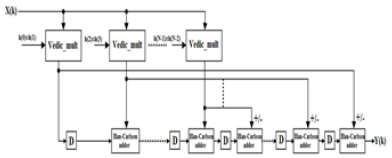

Fig. 4: Implementation of the subfilter-1 block

The subfilter-2 block contains the coefficient set with the length N/L. Hence it contains N/L vedic multiplier, N/L-1 Han-Carlson adder. Efficiency of the proposed filter depends on the performance of the multiplier and adder block. They are described as follows:

A. Vedic multiplier using BEC unit

Vedic multiplier used in the proposed architecture consumes less power and reduce the delay of the system. In this paper recently developed 16 * 16 bit vedic multiplier based on Urdhva-Tiryakbhyam formula [12] is used. It contains the 8 * 8 bit vedic multiplier, one 8 bit carry save adder, one 8 bit BEC (binary to excess-1 converter) and one multiplexer unit in the design. The design uses the BEC unit to achieve the lower area and power consumption. The main advantage of the BEC logic is the use of lesser number of the logic gates as compare to the n-bit full adder. In 16 * 16 bit multiplication multiplier size of P0 and P1 is 16 bit. P0 and P1 further divided into chunks of size n/2 = 8 bit, and fed to the input of 8 * 8 bit vedic multiplier module. Again these Chunks are repeatedly divided to get the chunk size of 2.

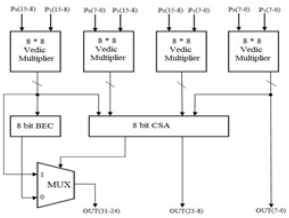

Fig. 5: 16 * 16 bit vedic multiplier using BEC

B. Han-Carlson adder

Han-Carlson adder has the advantage of higher speed execution at lower power and hardware utilization. In this design, Han-Carlson adder [13] follows the prefix processing. In the pre-handling stage the generate Gi and propagate Pi signal are calculated as:

$$\begin{aligned} G_i &= A_i ANDB_i \\ P_i &= A_i XORB_i \end{aligned} \tag{7}$$

The concept of generate and propagate signal further extended to blocks of adjoining bits, from bit k to bit i (with k< i) as follows:

$$G_i = G_{i-1} OR(G_{i-2} ANDP_{i-1})$$

$$P_i = P_{i-1} AND P_{i-2} \tag{8}$$

In the post processing stage, the final carry values obtained from the above subset used to calculate the approximate sum bits S_i. The post-processing unit is included adder and XOR gates. Final Sum is calculated as

$$S_i = P_i XOR G_{i-1:0} \tag{9}$$

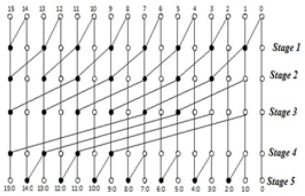

Fig. 6: 16 bit Han-Carlson adder

4 SYNTHESIS AND SIMULATION RESULTS

Synthesis results of 2 and 3 parallel symmetric FIR filter is shown in fig. 7. Complete RTL view of proposed 2-parallel design and subfilter-1 block are shown in fig. 8 and fig. 9 respectively. Simulation results of the 2 and 3 parallel symmetric FIR filter are shown in fig. 10 and fig. 11 respectively. Simulation of proposed parallel symmetric FIR filter based on FFA is done on Xilinx ISE simulator ISIM P.28xd. The coefficient of symmetric low-pass FIR filter of order 24 and 72 are generated by MATLAB. The set of subfilter block coefficients and input signal of word length 16 bit are also computed through MATLAB.

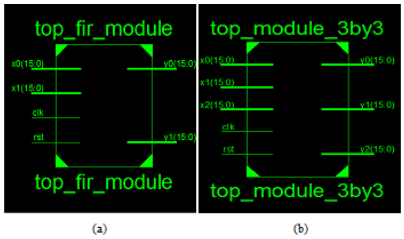

Fig. 7: Synthesis result of (a) 2-by-2; (b) 3-by-3 symmetric FIR filter

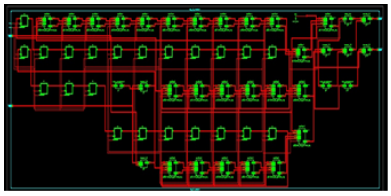

Fig. 8: RTL view of complete proposed 2-by-2 design

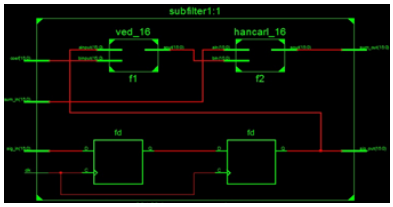

Fig. 9: Synthesis result of subfilter-1 block

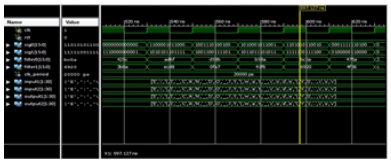

Fig. 10: Simulation results of 2-by-2 FIR filter

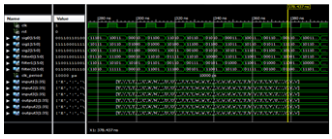

Fig. 11: Simulation results of 3-by-3 FIR filter

5 OF PROPOSED DESIGN

The proposed digital FIR filter architecture is designed through VHDL as a hardware description language and implementation is done on Xilinx ISE design suite 14.2. Design summary of the 2-by-2 and 3-by-3 proposed design for 24 and 72 order FIR filter is shown in fig. 12, fig. 13, fig. 14 and fig. 15 respectively.

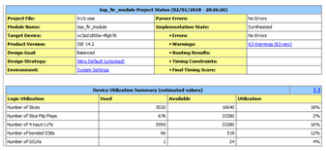

Fig. 12: Synthesis results of 2 by 2 FIR filter of 24 order

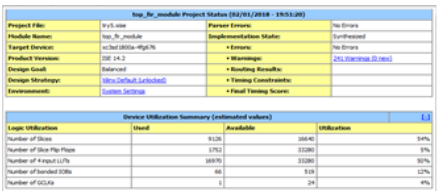

Fig. 13: Synthesis results of 2 by 2 FIR filter of 72 order

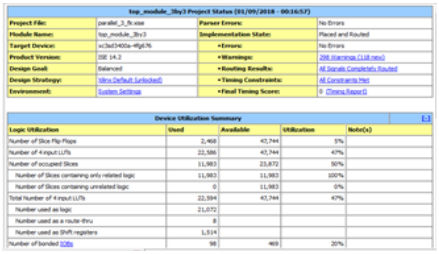

Fig. 14: Synthesis results of 3 by 3 FIR filter of 24 order

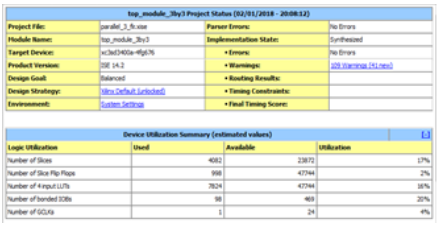

Fig. 15: Synthesis results of 3 by 3 FIR filter of 72 order

The power and timing analysis of different designs for 2 and 3 parallel digital FIR filter architecture are shown in table I and table II respectively. Table: II compares the critical path delay of proposed architecture with the conventional design.

TABLE I: Power analysis (Watt)

Length	L= 2	L= 3
FIR(24 tap)	0.130	0.201
FIR(72 tap)	0.139	0.217

TABLE II: Timing analysis (ns)

Length	Structure	L= 2	L= 3
FIR(24 tap)	FFA [10]	4.3	5.07
	Proposed	1.737	1.922
FIR(72 tap)	FFA [10]	9.68	9.92
	Proposed	3.921	4.326

6 CONCLUSION

In this paper, fast FIR algorithm based parallel symmetric FIR filter using Han-Carlson adder and vedic multiplier is proposed. The recently developed vedic multiplier with BEC unit and Han-Carlson adder used in the proposed design provides the advantage of higher speed and low hardware. The implementation results show that the proposed architecture reduces around 55% critical path delay over the conventional design. It also saves area requirement for the structure and shows acceptable performance. Due to low propagation delay and hardware, proposed architecture is useful in many signal processing and modern communication applications.

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