

MODELLING AND ANALYSIS OF MODIFIED BAUGH-WOOLEY MULTIPLIER USING GATE DIFFUSION INPUT AND IMPROVED SHANNON ADDER

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Abstract: As a crucial part of the Digital Signal Processor, a multiplier plays a major role in performing calculations within the processor. An important part of the electronic circuits in digital electronics is a binary multiplier which is capable of multiplying two binary digits. Most of the techniques developed for the purpose of multiplication involve calculation of the partial products separately and finally summing them to produce the multiplication output. This is the reason why a number of methods and technologies have been designed to make this multiplication process easier, minimizing the delay and error present. A comparative note on analysing CPL, Gate-Diffusion Input (GDI) and improved Shannon Adder technique is also made to determine the technique that uses minimum power when used as a full adder and GDI is found to be the optimum technique. This method uses CPL and Gate-Diffusion Input technique to implement an array multiplier and a modified Baugh-Wooley multiplier. However, a new Technique of improved Shannon Adder led to the implementation of the multipliers, resulting in better performance parameters. A comparative analysis on the power consumed and propagation delay is made with the help of Tanner EDA tool and it is found that Improved Shannon Adder implemented in modified Baugh- Wooley multiplier performs better than its peers.

Keywords: Baugh-Wooley Multiplier, GDI, Shannon Adder, CPL

1. Introduction

An important part of the electronic circuits in digital electronics is a binary multiplier which is capable of multiplying two binary digits. There are a number of methods with which a binary multiplier can be implemented. Most of the techniques developed for this purpose involve calculation of the partial products separately and finally summing them to produce the multiplication output. The method followed is similar to that of the long multiplication on base-10 integers, with slight modification to implement it in the base-2 number system. As a crucial part of the DSP, a multiplier plays a major role in performing calculations within the

processor. Typical DSP applications in which multipliers play a significant part include spectral analysis, digital communication and digital filtering.

2. Literature survey

A. Complementary Pass Transistor Logic (CPL):

A full adder implemented with complementary pass transistor logic involves the use of 32 transistors. The CPL full adder has been introduced to overcome the complexity issues that are included while using full CMOS pass gate logic. It dramatically decreases the number of gates used and further improves efficiency by using pure NMOS pass transistor [1]. The idea behind this method of full adder is to implement the operation with the help of NMOS pass transistors only. Hence, there is no inverter used to find the complementary form, hence the complementary inputs are manually given with direct input nodes.

B. Gate Diffusion Input:

A novel technique that is highly utilized for low power circuit design is the gate diffusion input technique. It allows a significant reduction in area, delay and power consumption of the circuit. The technique reduces the number of transistors used by using its gate as well as drain terminal as inputs rather than its typical function of being connected to the power supply and ground. By making optimum utilization of the available input terminals, the Gate Diffusion Input techniques, makes maximum use of what is available without including extra gates or devices to accomplish the purpose. A number of basic gates such as AND gate and OR gate can be devised with the GDI technique without using more than 2 MOS devices. The fig.1 shows the operation of a 2-bit adder with sum and carry with the help of Gate Diffusion Input technique.

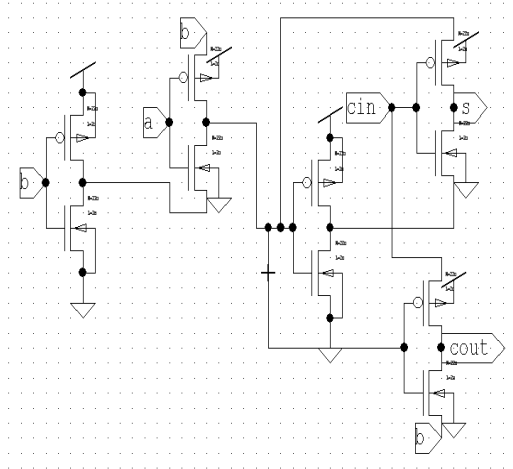


Figure 1. Schematic of Adder using Gate Diffusion Input

C. Improved Shannon Adder:

On drawing a Karnaugh's map of the full adder circuit, it can be further as Boolean expressions for the sum and carry signal. The expressions are given as

$$S = ABCin + A'B'cin + A'B'cin + AB'cin \quad (1)$$

$$Cout = AB + BCin + ACin \quad (2)$$

With the help of the above equations the pass transistor function can be performed. The output is the complement of the input when the expression gives '0'. Similarly, if it is '1', the input is given by the pass transistor function. When there are 'i' number of stages, the sum and cout of the i^{th} stage can be found using the formula

$$Cout_{i+1} = A_i B_i + (A_i \text{ xor } B_i) Cout_i \quad (3) \quad S_i = A_i \text{ xor } B_i \text{ xor } C_i$$

Based on Shannon's theorem, there are two ways in which a logic expression can be divided. When a variable is set to '0' and multiplying it by the inverse of the variable and when the variable is set to '1' and multiplying it by the variable.

$$F(a_0, a_1, a_2, \dots, a_n) = a_i F(a_0, a_1, a_2, \dots, a_n) + a_i' F(a_0, a_1, a_2, \dots, a_n) \quad (4)$$

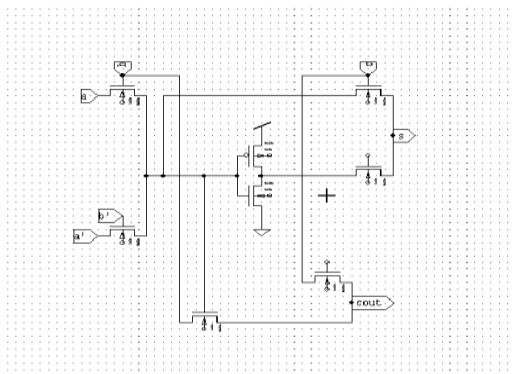


Figure 2. Schematic of Adder using Improved Shannon Adder

3. Proposed Method

There are a number of multipliers devised from early stages, starting with the array multiplier. A typical array multiplier can be implemented with the help of full adders and AND gates. The partial products are calculated using the AND gates and the output is obtained on summing with the help of full adders. Its regular structure is its advantage, but the delay prohibited is large. On moving up the ladder of multipliers, the Wallace tree multiplier is an important iterative realization of parallel multipliers for increased input bits. The modified Baugh-Wooley multiplier is the latest multiplier devised based on two's complement signed numbers. Each partial product is to be added in the form of a signed number. To avoid dealing with negative weights, an efficient method of adding bits to the bit matrix is proposed in this method. There are two cells that are used in the modified Baugh-Wooley multiplication namely the white cell and the grey cell. Two inputs are fed to an AND gate which is further fed along with a sum and carry bit into a full adder. This makes up the white cell. On the other hand, the grey cell implements a similar process with the help of NAND gate in the place of AND gate.

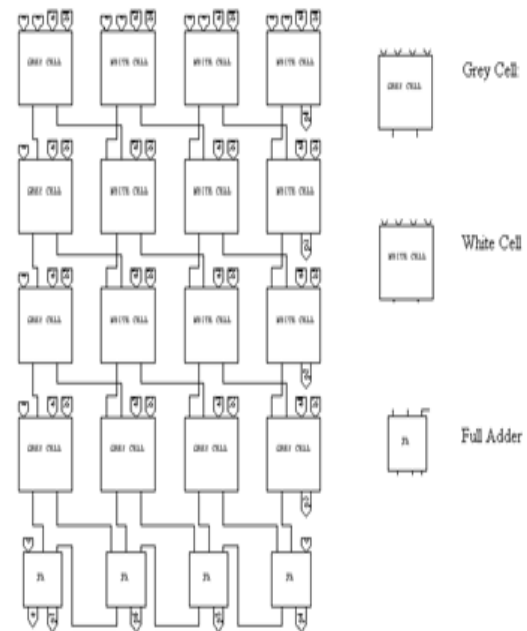


Figure 2. Modified Baugh-Wooley Multiplier

4. Simulation and Analysis

Simulation and Analysis are carried out with the help of Tanner EDA Tool.

A. Simulation Environment

The Simulation is done with 90 nm technology in Tanner EDA Tool and implemented in the same. The same input pattern has been given to all the multipliers to make the impartial testing environment. Design, verification and layout of mixed, as well as Analog signal is possible with the help of Tanner EDA. Waveform probing is done by W-Edit, schematic capture is accomplished by S-Edit and

Design entry and simulation system is done with T-Spice Pro.

B. Performance Analysis

A comparison is drawn on the techniques that can best implement the full adder. The techniques tested are CPL, GDI and Improved Shannon Adders. It is found that Improved Shannon Adder consumes less amount of power as seen from Table 1. The multipliers designed are implemented with GDI technique and are compared in terms of power and delay. It is found that the modified Baugh-Wooley multiplier is the optimum multiplier used.

Table 1. Performance Analysis of Multipliers

ADDER TYPE	MULTIPLIER	POWER CONSUMPTION (Watts)	PROPAGATION DELAY (ns)
CPL LOGIC	ARRAY	0.6570	1.64
	MODIFIED BAUGH-WOOLEY	0.5980	1.45
GDI TECHNIQUE	ARRAY	0.5373	1.34
	MODIFIED BAUGH-WOOLEY	0.4983	0.87
IMPROVED SHANNON ADDER	ARRAY	0.5398	1.20
	BAUGH-WOOLEY	0.4925	0.84

The Improved Shannon Adder simulation result is as given in Fig. 3.

Fig. 3 Improved Shannon Adder Simulation Result

5. Conclusion

The 4-bit multiplier designed can handle signed multiplication. Testing of the multiplier is done with Tanner EDA. The modified Baugh-Wooley algorithm is used to reduce the cumulative gate delay that otherwise forms in other multipliers. In addition, the algorithm uses common logical units to simplify design and deals with signed inputs more efficiently than other algorithms. This produces a relatively efficient calculation time, while maintaining low-cost production costs. Although the algorithm is not able to work with unsigned inputs, the goal of the project was signed multiplier.

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