

An MFA Binary Counter for Low Power Application

Sneha P
Department of ECE
PSNA CET, Dindigul, India

Dr. M. Thiruvani
Department of ECE
PSNA CET, Dindigul, India

ABSTRACT- Counters are used to determine how many of the inputs are active (in the logic ONE state) for multi input circuits. Counters are widely used in a variety of applications. In the existing systems 6:3 and 7:3 Counters are designed which uses 3-bit stacking and 6-bit stacking circuits which group all the "1" bits together and the stacks are converted into binary counts. This leads to higher power consumption and increased area. To overcome this problem "MUX based Full adder" 6:3 and 7:3 counters are proposed. In addition to enhance the reliability of the counter, Triple Modular Redundancy fault tolerant technique is proposed. The counter architecture is coded in Verilog HDL and synthesized in Xilinx 12.1. From the synthesized result the area, power and delay for the counter is analyzed.

KEY WORDS- Stacking Circuits, MUX based full adder, Triple Modular Redundancy (TMR)

1. INTRODUCTION

With the ever-increasing applications in mobile communications and portable equipment, the demand for low-power VLSI systems is steadily increasing. Binary counters are key elements in many arithmetic circuits. An (n,m) binary counter is a circuit with n inputs that produces an m-bit binary count of the number of its inputs that are ones. A binary counter may be viewed as a multiple word input adder with 1-bit word length. Counters applications include in the realization of multipliers, computer arithmetic units, multiple input adders and associative processors. Counters are also used in digital neural networks. Counters play an important role in multipliers. Multiplier circuits are an essential part of an arithmetic logic unit or a digital signal processing system for performing filtering and convolution. The binary multiplication of integers or fixed-point numbers results in partial products that must

be added to produce the final product. The addition these partial products increases the delay and power consumption of the multiplier. Hence the counters are used in reducing the partial products and reduces the delay and power consumption. Counters The different type of binary counters used are threshold gate counters,

switching tree counters, Carry shower counters, Successive doubling counters, Quasi digital counters.

A. RELATED WORKS

In existing system, the full adder counters, fast adder counters, quasi digital techniques. The full adder counter is modified such that it uses only Read Only Memories (ROM) are called adder counters. The quasi digital counters are used to generate an analog signal proportional to the count which is the digitized. The full adder counter is slower than the fast adder counter, while quasi digital counter appears to be proportionally faster the above two counters [2]. From this basis a 3-2 and 4-2 counter are designed which are the basic components in the partial product summation tree of a parallel array multiplier [3]. These counters are realized using XOR/XNOR gates which are implemented using the Double Pass Transistor logic (DPL) circuit technique. 4-2 counters are implemented using 6 DPL MUXs. By using MUX in this logic, the internal node capacitance on the critical path is reduced which paved the way for the "MUX based Full Adders". Also, the counters are designed using the Pass transistor and the Transmission gates. The counter comprises of the CMOS pass network XOR-XNOR cell which can reliably operate within certain bounds when the power supply voltage is scaled down. The 7:2 counters are designed with the XOR gates in which the critical path delay equals to 6 XORs [4]. Further with the use of 2:2, 3:2, 4:3, 5:3, 6:3 and 7:3 counters are used in the partial product reduction of multipliers.

B. SYMMETRIC STACKING COUNTERS

The symmetric stacking counters uses 3-bit stacking circuits, which group all of the “1” bits proceeded by a symmetric method to incorporate pairs of 3-bit stacks into 6-bit stacks [1].

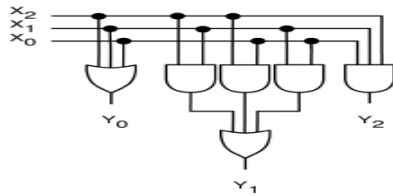


Fig 1. Three-bit stacking circuit

The bit stacks are then transformed to binary counts. Given inputs X_0 , X_1 and X_2 a 3-bit stacker circuit shown in Fig 1 will have three outputs Y_0 , Y_1 and Y_2 such that the number of “1” bits in the outputs is the same as the number of “1” bits in the inputs, but the “1” bits are grouped together to the left followed by the “0” bits. The outputs are formed by

$$Y_0 = X_0 + X_1 + X_2$$

$$Y_1 = X_0X_1 + X_0X_2 + X_1X_2$$

$$Y_2 = X_0X_1X_2$$

Namely, the first output will be “1” if any of the inputs is one, the second output will be “1” if any two of the inputs are one, and the last output will be one if all three of the inputs are “1”. The Y_1 output is a majority function and can be implemented using one complex CMOS gate. In the same way the six bit stacking circuits are used to group the one bits together.

C. SYMMETRIC STACKING 6:3 COUNTERS

To implement a 6:3 counter the bits stacks are to be converted to the binary number. The 6:3 counter is shown in Fig 2.

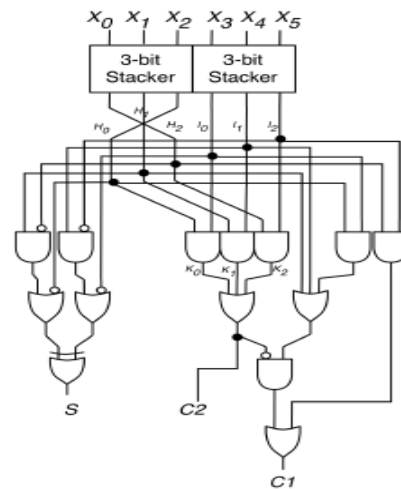


Fig 2. Symmetric 6:3 Counter

For the faster, more efficient count, we can use intermediate values H , I and K to quickly compute each output bit without needing the bottom layer of stackers. The output bits C_2 , C_1 and S in which C_2 , C_1 and S is the binary representation of the number of “1” input bits.

$$H_e = \overline{H_0} + \overline{H_1}H_2$$

$$I_e = I_0 + I_1I_2$$

$$S = H_e \text{ XOR } I_e$$

$$C_1 = (H_1 + I_1 + H_0I_0)(K_0 + \overline{K_1} + K_2) + H_2I_2$$

$$C_2 = K_0 + K_1 + K_2$$

To compute S , we note that we can easily determine the parity of the outputs from the first layer of 3-bit stackers. Even parity occurs in the H if zero or two “1” bits appear in X_0 , X_1 and X_2 .

D. SYMMETRIC STACKING 7:3 COUNTER

The symmetric stacking method can be used to create a 7:3 counter involves computing outputs for C_1 and C_2 assuming both $X_6 = 0$ (which matches the 6:3 counter) and assuming $X_6 = 1$. We compute the S output by adding one additional XOR gate.

$$C_1 = (H_0 + I_0)J_0J_1J_2 + H_2I_1 + H_1I_2$$

$$C_2 = J_0J_1J_2$$

Both versions of C_1 and C_2 are computed and a MUX is used to select the correct version based on X_6 . This design consists of more number of XOR gates on its critical path. Hence the critical path delay is increased in this design. This leads to higher power consumption. The symmetric 7:3 counter is shown in Fig 3.

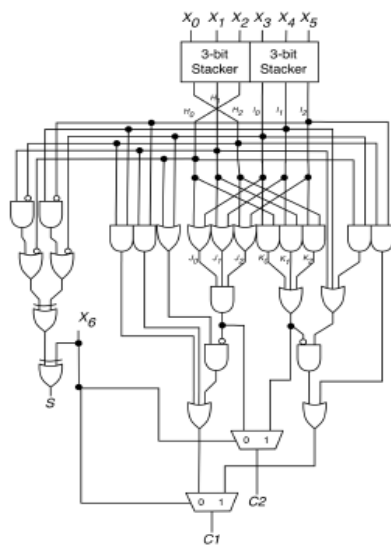


Fig 3. Symmetric 7:3 counter

These counters are then implemented in the Wallace tree multiplier. On the analysis of the results of these counters the area and power consumption are increased when compared with the conventional counter techniques. In order to reduce the area and power consumption the “MUX based full adder” counter is designed.

2. PROPOSED METHOD

In this method a binary counter design is proposed which is designed with the MUX based Full adders. In order to reduce the power consumption and area of the existing counter design this method is proposed. MUX based Full adder 6:3 counters and 7:3 counters are designed and the fault detection scheme using the Triple Modular Redundancy is proposed. These methods involve using MUX based full adders functioning as counters to reduce groups of 3 bits of the same weight to 2 bits of the different weight.

E. MFA

The proposed MFA counter is shown in Fig 4. Which consists of two 2:1 MUX and an XOR gate. In the proposed structure, one XOR block in the conventional Full Adder is replaced by a multiplexer block so that the critical path delay is minimized. The critical path delay is given by,

$$\text{Delay} = \text{XOR} + \text{MUX}$$

This can be implemented by using second MUX with XOR output as a selection line. Since XOR employs most of the power consumption in the adder circuit, by reducing number of XOR gates, power consumption of the full adder can be reduced.

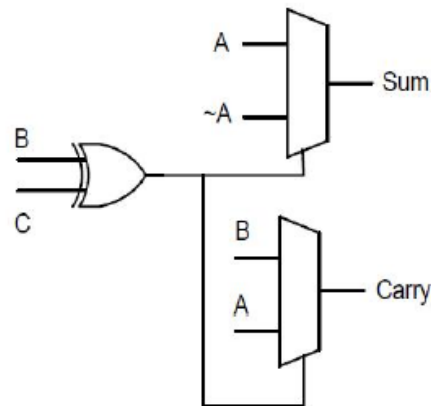


Fig 4. MUX based Full Adder

The proposed Full adder three bits are given as input. Out of the three inputs, one input and its complement are provided as inputs to the first multiplexer. The other two inputs are given to the XOR gate, the output of which will act as a select line to both the multiplexers. The inputs of the second multiplexer are, the bits other than the carry bit. This unique way of designing leads to the reduction of switching activity, which in turn reduces the power. In addition to this, the critical path delays also reduced compared to the existing designs in literature which leads to reduction in delay and thus increasing the speed. Operation of the Full adder is explained by the algorithm,

ALGORITHM

```

T = B XOR C
T = 0
Sum = A
Carry = B
T = 1
Sum = ~A
Carry = A

```

F. MFA 6:3 COUNTER

The MFA 6:3 counter is shown in Fig 5. Which consists of three MUX based Full adders and one-half adder. In this method the area, power and delay is reduced.

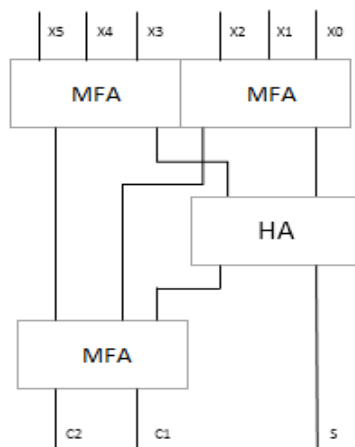


Fig 5. MFA 6:3 Counter

The inputs of the counter are given as $\{X_0, X_1, \dots, X_5\}$. The first three inputs X_0, X_1 and X_2 undergo the XOR operation. The result of the XOR operation is denoted as " t_0 ". The t_0 is given as the select lines for the two multiplexers. If the value of t_0 is 0 then for the sum output the value is X_0 , carry value is given by X_1 . If the value of t_0 is 1 then for the sum output the value is X_0 . The carry value is given by X_0 . Similarly, the next three inputs X_4, X_5 and X_6 is given to the next MFA. The first two inputs undergo XOR operation and the sum and carry are determined. The sum output from the first MFA and second MFA are given to the half adders and the operation is performed which gives the sum and carry output. For the third MFA all the carry outputs are given as inputs. The sum, carry1 and carry2 are generated at the third MFA.

G. MFA 7:3 COUNTER

The 7:3 counters are desirable in many applications as they provide higher compression ratio. The 7:3 counter circuit is shown in Fig 6. Which accepts 7 bits of equal weight and counts the number of 1 bits. This count is then output using three bits of increased weight.

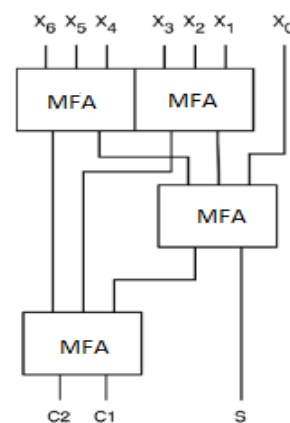


Fig 6. MFA 7:3 Counter

The MFA 7:3 Counter consists of 4 "MUX based Full adders". The 7-bit input are given as $\{X_0, X_1, \dots, X_7\}$. The inputs X_1, X_2 and X_3 are given to the first MFA. The X_2 and X_3 undergo XOR operation. The output of the XOR operation is denoted as " t_0 ". The " t_0 " is given to the select lines to the multiplexer. If " t_0 " is 0 then sum is X_1 and carry is X_2 . If " t_0 " is 1 then sum is X_1 and carry is X_2 . Similarly, for all the Full adders the input is given and the output is obtained using the select lines. The fourth MFA gives the sum, carry1 and carry2 outputs. Which results the binary count of the given input. The 7:3 counters gives higher compression ratio and hence it is used in many multipliers for the partial product reduction.

H. FAULT DETECTION USING TMR

A fault is an unattractive or unsatisfactory feature especially in a piece of work or in a circuit that may lead to undesirable changes in the output. Hence fault detection and correction is one of the important issue in designing a circuit. To meet the reliability requirements such circuits should be equipped with appropriate error detection and correction mechanisms. One of the well-known and widely used fault tolerant techniques in safety critical applications is Triple Modular Redundancy (TMR) [5]. The fault detection using TMR is given in fig 7.

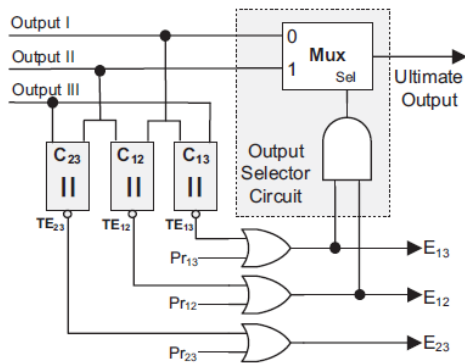


Fig 7. Fault detection using TMR

The TMR system consists of three redundant modules and a voter at the modules output. A wrong detection or inability to locate the faulty module can significantly affect the system reliability. To address this issue a voter can also detect possible faults occurring in the comparators. As shown in fig 7. The comparators are used to represent the mismatch between the TMR modules. The voter can also detect the permanent faults, the proposed voter employs three input signals Pr_{12} , Pr_{13} and Pr_{23} . If ($Pr_{12}=Pr_{13}=Pr_{23}=0$) and as a result E_{12} , E_{13} and E_{23} become equal to TE_{12} , TE_{13} and TE_{23} respectively. The output selector uses E_{12} and E_{13} signals as inputs of a logical AND gate to generate the select signals for a 2:1 multiplexer. In the proposed voter, an output selector is used to route the error free output to the ultimate output signal.

3. SIMULATION RESULTS

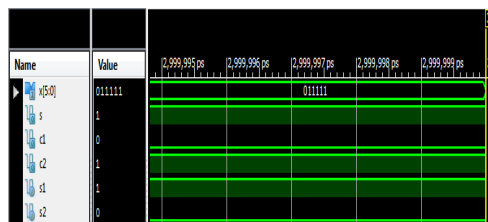


Fig 9. MFA 6:3 Counter

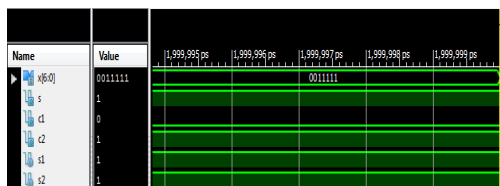


Fig 10. MFA 7: 3 Counter

4. SYNTHESIS REPORT

nfascnthree Project Status (10/16/2017 - 14:53:06)			
Project File:	nfascnthree.vise	Parser Errors:	No Errors
Module Name:	nfascnthree	Implementation State:	Synthesized
Target Device:	xc3s100e-Spg100	Errors:	No Errors
Product Version:	ISE 12.1	Warnings:	7 Warnings (0 new)
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Vlrox Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	960	0%
Number of 4 input LUTs	3	1920	0%
Number of bonded IOBs	8	66	12%

Fig 11. MFA 6:3 Counter

nfascoun Project Status (10/13/2017 - 09:09:59)			
Project File:	nfascoun.vise	Parser Errors:	No Errors
Module Name:	nfascoun	Implementation State:	Synthesized
Target Device:	xc3s100e-Spg100	Errors:	No Errors
Product Version:	ISE 12.1	Warnings:	4 Warnings (4 new)
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Vlrox Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4	960	0%
Number of 4 input LUTs	8	1920	0%
Number of bonded IOBs	10	66	15%

Fig 12. MFA 7:3 Counter

5. COMPARISON TABLE

	DELAY(ns)		SLICE		POWER(W)	
	6:3	7:3	6:3	7:3	6:3	7:3
Symm. Counter	7.23	9.535	5	9	0.088	0.116
MFA Counter	6.897	7.981	2	4	0.067	0.081

6. PERFORMANCE ANALYSIS

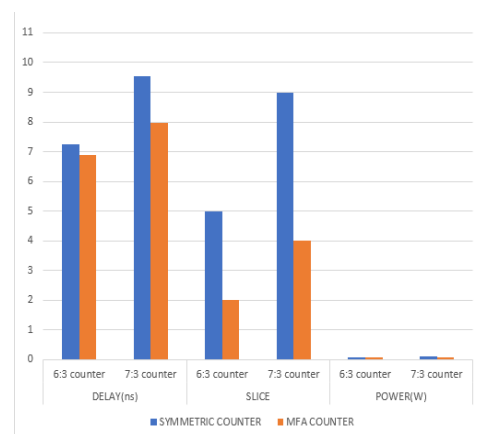


Fig 13. Comparison Graph

7. CONCLUSION

In the existing system 6:3 and 7:3 counters are designed using symmetric stacking method. In the proposed system, the MFA based 6:3 and 7:3 counter is designed which is area effective and speed efficient. In

this method, the power consumption is also reduced when compared to the existing system. The power consumption is reduced by 23.863% and 16.297% for 6:3 and 7:3 counters respectively. The area is given in terms of slice which is reduced by 60% and 55.5% for the 6:3 and 7:3 counters respectively. The delay is reduced by 4.698% and 16.297% for the 6:3 and 7:3 counters respectively. These results are compared with the symmetric stacking 6:3 and 7:3 counter.

8. REFERENCES

1. Christopher Fritz, Adly T Fam (2017) "Fast binary counters based on symmetric stacking" IEEE Trans VLSI Systems., pp. 1-5.
2. Swartzlander, E E., Jr., (1973) "Parallel Counters" IEEE Trans. Computers, Vol. 22, pp 1021-1024.
3. S F Hsiao, M R Jiang and J S Yeh (1998) "Design of high speed low power 3-2 counter and 4-2 compressor for fast multipliers" Electron Lett., Vol.34, no. 4, pp.341-343.
4. D Radhakrishnan, (2001) "Low voltage low power CMOS Full Adder" IEEE Proc-Circuits, Devices Syst., Vol.148, no.1, pp.19-24.
5. G Latif, Shabgahi and S Bennett, (1999) "Adaptive memory voter-A novel voting algorithm for real time fault tolerant control systems" in proc. 25th EUROMICRO Conf., Vol.2, pp.113-120.

