VLSI BASED 64-POINT PIPELINED FFT USING RADIX-4 COMBINED SDF-MDC

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Abstract
This paper presents the design of new VLSI based 64-point pipelined Radix-4 FFT architecture named as "64-point pipelined FFT using Radix-4 Combined Single Path Delay Feedback (SDF) - Multi path Delay Commutator (MDC) FFT". As the name itself indicates, the design of proposed FFT architecture is designed with the help of both SDF and MDC structures that have different types of advantages based on their data flow structures. SDF structure has advantages in improving the speed and MDC structure has advantages in reducing the low chip area and lower power consumption. In addition to the developed architecture, Modified Bit Parallel Multiplier (MBPM) has been used in the place of twiddle factor multiplication. When compared to traditional equivalents, the proposed architecture which is used to improve the high processing speed and high performances of FFT processor. Simulation of proposed FFT architectures are evaluated by using ModelSim 6.3C and performances are validated by using Xilinx Plan-ahead Integrated Circuit (IC) vendors. Proposed new circuits will be absolutely used in Orthogonal Frequency Division Multiplexing (OFDM) and Software Defined Radio (SDR) system.

Keywords: Mixed Radix Architecture, Fast Fourier Transform, Combined SDF-MDC Architecture, Look Up Tables, less area utilization

1. Introduction
Wireless communication technology has enlarged the demands for signal processing operations such as Convolution, Correlation, Filtering and frequency transformation techniques. Among those kind of operations, Fast Fourier Transformation (FFT) i.e. frequency transformation technique is recognized as a high potential for wireless based communication in terms of hardware complexity.

In general, FFT is widely used to convert the frequency domain signal into time domain signal and Inverse Fast Fourier Transformation (IFFT) is widely used to convert the time domain signal into frequency domain signal. These frequency transformation techniques are used to transmit and reconstruct the original input signals in OFDM based communication. For instance, Mobile Ad-hoc Network (MANET) is the type of infra-structure less wireless network in which OFDM is used to transmission of information signals to desired users. OFDM is a multi-carrier transmission scheme in which higher rate single data stream is transmitted over a number of lower sub-carriers.

To analyse and transmit the frequency characteristics of more number of lower rate data streams, FFTs and IFFTs are generally used. FFT/IFFT blocks consume more silicon area and power consumption. Also, Speed of frequency transformation processes is also poor due to difficult signal flow graph. In this research work, pipelining mechanism is introduced to increase the speed of the FFT/IFFT processors. In addition to pipelining process, reduced complex multiplier is designed to reduce the hardware cost and power consumption of the FFT/IFFT processors.

We need to perform N multiplications and N-1 additions for an N-point DFT. Therefore, there will be complex multiplications of N2 and complex additions of N (N-1). Different platforms such as computer chips and general purpose processors are implemented by the Fast Fourier Transform (FFT).FFT uses a divide and conquer methodology for its computation process. This divides the N co-efficient into smaller blocks in different stages. Single path Delay Feedback (SDF) FFT processors are used to increase the speed of the frequency transformation processes. Multi-path Delay Commutator (MDC) architecture reduces the hardware slices and power consumption of the FFT processors.
The N-point DFT of an input sequence is defined as

\[ X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}, \quad 0 \leq k \leq N - 1 \]

\[ W_N^{kn} = e^{-j2\pi kn/N} \]

When N is a power of two, the FFT based on the Cooley–Tukey algorithm is most commonly used in order to compute the DFT efficiently[1]. The Cooley–Tukey algorithm reduces the number of operations (N^2) for the DFT to (N log_2 N) for the FFT. In accordance with this the FFT calculated in a series of n = log_p N stages where p is the base of the radix. The other popular algorithm is the radix-4 FFT, which is even more efficient than the radix-2 FFT. The radix-4 FFT equation is listed below:

\[ x(4k_1 + l) = \sum_{k=0}^{N} x(n) + x(n + N/4) W_4^l + x(n + N/2) W_4^{2l} + x(n + 3N/4) W_4^{3l} W_N^{Nk_1} \]

(l = 0, 1, 2, 3; k_1 = 0, 1, 2, 3 ... N/4 - 1)

The radix-4 FFT equation essentially combines two stages of a radix-2 FFT into one, so that half as many stages are required. Since the radix-4 FFT requires fewer stages and butterflies than the radix-2 FFT the computations of FFT can be further improved. For example, to calculate a 16-point FFT, the radix-2 FFT takes \log_2 16 = 4 stages but the radix-4 FFT takes only \log_4 16 = 2 stages[2-4].

![Figure 1 Architecture of Radix-4 FFT](image)

**EXISTING METHOD**

**EXISTING RADIX-4 MULTIPATH DELAY COMMUTATOR**

Multi-path Delay Commutator (MDC) architecture reduces the hardware slices and power consumption of the FFT processors than Single path Delay Feedback (SDF). The architecture of Radix-4 Multi-path Delay Commutator (R4MDC) FFT has been illustrated in figure 2. As shown in architecture of R4MDC, input data is shifted according to their appropriate delay positions. Commutator unit is used to re-arrange the one form of signals into another form of signal. On the other hand Butterfly unit is used to add and subtract the signed bit values. Appropriate delays are used to determine proper frequency response in appropriate delay positions. If there is more number of samples are included in FFT processes, signal strength should be increased while performing data communication [5-7].
Due to merging the real and imaginary values of complex input values, it is possible to reduce the half of the accumulation and subtractor units while calculating FFT processes [8]. However, it requires more delay for exhibiting frequency transformation process.

EXISTING RADIX-4 SINGLE PATH DELAY FEEDBACK

Single path Delay Feedback (SDF) FFT processors are used to increase the speed of the frequency transformation processes. When compared to MDC FFT processors, SDF FFT processors use less critical path to find the frequency transformation process. The architecture of 16-point Radix-4 Single path Delay Feedback (R4SDF) FFT has been illustrated in figure 3.

As shown in figure 3, architecture of 16-point R4SDF FFT has only two stages whereas architecture of 16-point R2SDF FFT has four stages. Hence, speed of SDF based FFT processors have been improved significantly rather than MDC FFT processor [9]. But, SDF processors do not support in reducing the hardware slices and power consumption. Bit Parallel Multiplication (BPM) structure has been used in R4SDF architecture [10]. For instance, three most twiddle factor values are used in frequently such as 0.9239, 0.3827 and 0.707.

2. Research Method

PROPOSED MIXED ARCHITECTURE
In this paper, advantages of different pipelining architectures such as SDF and MDC are analyzed and re-designed by using Radix-4 Mixed architecture for utilizing advantages of both architectures. The advantages and disadvantages of SDF and MDC data-flow structures are listed in Table 1.

<table>
<thead>
<tr>
<th>Architecture Types/Parameters</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single path Delay Feedback</td>
<td>High Speed</td>
<td>More hardware slice and power utilization</td>
</tr>
<tr>
<td>Multipath Delay Commmutator</td>
<td>Less hardware slice utilization and lower power consumption</td>
<td>Low speed</td>
</tr>
</tbody>
</table>

Table 1 Advantages and Disadvantages of SDF and MDC data flow structures

From above two columns of the table, we identify the problems of different types of architectures and designed a new data flow structure which combines both SDF and MDC flow graphs. Radix-4 FFT has been implemented in this paper for reducing the number of stages and twiddle factor multiplications. The structure of proposed Radix-4 Mixed SDF-MDC architecture has been illustrated in figure 4.

**Figure 4 Architecture of proposed Mixed SDF-MDC data flow structure**

PROPOSED 64-POINT PIPELINED RADIX-4 FFT

The below Fig. 5 shows the signal flow graph of 64-point radix-4 FFT and the general structure of the radix-4 butterfly. For hardware realization of FFT, multi-bank memory and “in place” addressing strategy are often used to speed-up the memory access time and minimize the hardware consumption. For radix-r FFT, r banks of memory are needed to store data, and each memory bank could be two-port memory. With “in-place” strategy, the r outputs of the
butterfly can be written back to the same memory locations of the r inputs, and replace the old data. In this case, to realise parallel and pipelined FFT processing, an efficient addressing scheme is needed to avoid the data conflict. A popular addressing scheme for radix-\(r\) (\(r>2\)) was presented by Johnson, however due to the modulo-\(r\) addition, this method is slow and the speed depends on the length of FFT.

3. Results and Analysis

The proposed design of 64-point pipelined Radix-4 SDF-MDC FFT has been made by using Verilog. The simulation results have been evaluated by using ModelSim 6.3c and Synthesis Performances are estimated by using Xilinx 10.1i (Package: pq208, Family: Spartan-3, Device: Xc3s200) design tool. The simulation result of proposed 64-point pipelined Radix-4 SDFMDC FFT is illustrated in Fig.6. In the place of twiddle factor multiplication, Bit Parallel Multiplication (BPM) has been used in this research work. Bit Parallel Multiplication (BPM) consists of only shifters and adders to perform twiddle factor multiplication operation. The twiddle factor values stored in RAM memory for the design of 64-point FFT the data flow structure of Proposed SDF architecture and the data flow structure of Proposed MDC architecture are studied. In addition, structure of BPM has been modified by reducing the unwanted shifters and adders. Hence, it is further having possibilities to reduce the hardware complexity.
3.1. Comparison of existing and proposed methods

The performance evaluation of existing 64-point Radix-4 FFT and proposed 64-point pipelined Radix-4 SDF-MDC FFT are analyzed and compared in Table 2.

Table 2 Comparison of existing 64-point Radix-4 FFT and proposed 64-point pipelined Radix-4 SDF-MDC FFT

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Existing 64-point Radix-4 FFT</th>
<th>Proposed 64-Radix-4 SDF-MDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUTs</td>
<td>10,317</td>
<td>1768</td>
</tr>
<tr>
<td>Slices</td>
<td>5732</td>
<td>1058</td>
</tr>
<tr>
<td>Delay(ns)</td>
<td>14.188ns</td>
<td>12.875ns</td>
</tr>
<tr>
<td>Power(w)</td>
<td>6.093w</td>
<td>2.290w</td>
</tr>
</tbody>
</table>

3.2. Performance evaluation of existing and proposed methods

The performance evaluations are graphically illustrated in Fig. 7.

From [Table 2] and Fig.7, it is clear that proposed 64-point pipelined Radix-4 SDF-MDC FFT offers 81.54% reduction in hardware slices, 82.86% reduction in number of LUTs, 9.25% reduction in delay and 62.41% reduction in power consumption than the existing 64-point Radix4 FFT. When compared to existing method, the numbers of occupied slices are 5732 which is reduced to 1058, the total number of LUTs are 10,317 which is reduced to 1768, the
4. Conclusion

64-point pipelined Radix-4 Single path Delay Feedback (SDF) – Multiple path Delay Commutator (SDC) FFT has been proposed through Very Large Scale Integration (VLSI) System design environment. The main aim of this paper is to reduce the processing time and improve the speed of the FFT processor. The proposed method used to reduces the slices, LUTs, delay and power consumption. The proposed 64-point pipelined Radix-4 SDF-MDC FFT offers 81.54% reduction in hardware slices, 82.86% reduction in number of LUTs, 9.25% reduction in delay and 62.41% reduction in power consumption than the existing 64-point Radix-4 FFT. In future, the proposed architecture will absolutely be useful in OFDM based digital communication to perform the function of frequency transformation and to analyze the spectrum characteristics of digital inputs.

References
