AN EFFICIENT APPROACH TO DELAY ESTIMATION MODEL FOR VLSI INTERCONNECT

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Abstract: In recent days there is huge demand for high speed VLSI networks. In order to judge the behavior of on-chip interconnects the coupling capacitances and interconnect delays plays a major role. As we switch to lower technology there is on-chip inductance effect that leads to interconnect delay. In this paper we try to apply second order transfer function designed with finite difference equation and Laplace transform at the source and load termination ends. Analysis shows that current mode signaling in VLSI interconnects provides times better delay performance than voltage mode.

Keywords: Current Mode, Voltage Mode, VLSI Interconnect

1. Introduction

As the number of transistors on a chip continues to increase, on-chip communication becomes a more important facet of architectural design. Traditional electrical wires, typically driven by digital components using simplistic digital signals have issues to address in the scaling chip multiprocessor market, specifically latency and energy. Global wire latency remains relatively constant, translating to a larger relative latency for even moderately-sized systems. In order to ensure signal quality, digital repeaters and packet-switching routers must be added to facilitate the transmission of long distance communications, contributing further to the latency and energy issues. Current research focuses on a few categories of solutions, each with unique benefits and limitations. The current convention is the use of packet-switching networks topologies to provide the interconnect backbone for chip-multiprocessors. A packet-switched network-on-chip (NoC) provides in-field scalability, the ability to use commercial-off-the-shelf components, and high aggregate throughput. However, a NoC also requires higher power routers and potentially long latencies for long distance communication. Another state-of-the-art solution for interconnects uses on-chip optics. Research is currently being proposed to use either waveguides or free-space optics to provide a high-throughput, low-energy, low-latency medium for on-chip communication. On the other hand, optics also has issues that prohibit its immediate use as an interconnect backbone.

2. Related Works

Signaling in global strains is a main bottleneck in excessive performance VLSI systems because of the dominant problem of signal propagation delays in comparison to circuit delays. Starting from lumped RC model to distributed RLC version, diverse techniques [6]-[8] based on analytical closed form formulations had been proposed to model delay in voltage-mode interconnects. Similarly for modern-day-mode RC interconnects, closed-form delay analysis version becomes presented in [9] and the evaluation does not encompass the fast aspect input reaction. In [10] closed-form delay model for allotted contemporary-mode RC line is provided. A delay estimation model [11], that's derived the use of the concept of soaking up inductance impact into equal RC version, then changed nodal evaluation (MNA) become used. Various closed-form delay models [9]- [13] for on-chip interconnects in present day-mode signaling have more inaccuracy in phrases of postpone estimation.

3. Finite Difference Equation And Laplace Transform

The Taylor series expansion for a function of one variable about the point x is
\[ f(x + h) = f(x) + hf'(x) + \frac{h^2}{2!}f''(x) + O(h^3) \ldots (1) \]

The notation O(h^3) indicates that the series, when truncated at the quadratic term in h, contains errors that scale as h^3 and higher powers of h.

\[ f'(x) = \frac{f(x + h) - f(x)}{h} + O(h) \ldots (2) \]

Note that, even though we neglect terms of O(h^2) in the expansion, since we divide through by h to obtain the derivative expression the approximation is correct to
O(h^1) only. Note that there is an asymmetry in this approximation to the derivative at x, since the function at x and x+h occur, but not the function at x-h. This is therefore referred to as a forward difference approximation. It is possible to expand f(x) in the negative direction in the Taylor expansion and hence to obtain a backward difference approximation

\[ f(x-h) = f(x) - h f'(x) + \frac{h^2}{2!} f''(x) + O(h^3) \]  

\[ f'(x) = \frac{f(x)-f(x-h)}{h} + O(h) \]  

\[ f(x+h) = f(x) + h f'(x) + \frac{h^2}{2!} f''(x) + O(h^3) \]  

\[ f(x-h) = f(x) - h f'(x) + \frac{h^2}{2!} f''(x) + O(h^3) \]  

\[ f(x+h)-f(x-h)=2h f'(x)+\frac{2h^3}{3!} f'''(x)+O(h^4) \]  

\[ f'(x) = \frac{f(x+h)-f(x-h)}{2h} + O(h^2) \]  

\[ h^2 f''(x) = f(x+h) - 2f(x)+f(x-h) + O(h^4) \]  

\[ f'''(x) = \frac{f(x+h)-2f(x)+f(x-h)}{h^3} + O(h^2) \]  

A. Taylor series expansions in more than one dimension

A PDE contains at least two independent variables and so we need to approximate differential operators in at least two dimensions. This is done using Taylor series expansions in more than one dimension. Suppose \( u = u(x,y) \)  

\[ u(x+h,y)=u(x)+h \nabla u(x)+\frac{1}{2!} h^2 \nabla \nabla u(x) \cdot h + O(h^3)^2 \]  

\[ h = \begin{pmatrix} h \\ k \end{pmatrix} \quad h^T = \begin{pmatrix} x \\ y \end{pmatrix} \quad \nabla \nabla = \frac{\partial^2}{\partial x_i \partial x_j} \]  

Returning to the long-hand notation, the expansion of \( u(x,y) \) in the x direction is

\[ u(x+h,y)=u(x,y)+h u_x(x,y)+\frac{h^2}{2!} u_{xx}(x,y)+O(h^3) \]  

If we subtract these two equations and rearrange to make \( u_x \) the subject of the equation we find that the central difference approximation to \( u_x \) is

\[ u_x(x,y) = \frac{u(x+h,y)-u(x-h,y)}{2h} + O(h^2) \]  

\[ u(x,y+k) = u_{i+1,j} \]  

\( k \) is the step size or distance between gridpoints in the y direction in the numerical solution.

\[ u_x(x,y) = \frac{1}{2h} \left( u_{i,j+1} - u_{i,j-1} \right) + O(h^2) \]  

\[ u_y(x,y) = \frac{1}{2k} \left( u_{i+1,j} - u_{i-1,j} \right) + O(k^2) \]  

\[ u_{xx}(x,y) = \frac{1}{h^2} \left( u_{i,j+1} - 2u_{i,j} + u_{i,j-1} \right) + O(h^2) \]  

\[ u_{yy}(x,y) = \frac{1}{k^2} \left( u_{i+1,j} - 2u_{i,j} + u_{i-1,j} \right) + O(k^2) \]  

\[ \nabla^2 u(x,y) = \frac{1}{k^2} \left( u_{i+1,j} - u_{i,j} + u_{i,j+1} + u_{i,j-1} - 4u_{i,j} \right) + O(h^2) \]  

4. Voltage mode interconnects

Voltage mode signaling is most widely used in VLSI chips. In voltage mode signaling, receiver provides high input impedance (ideally infinity). Fig.1 shows the theoretical model of conventional voltage mode interconnect implementation [5].

CMOS representation of voltage mode is shown in Fig. 2 [1, 3]. The driver consists of an inverter which drives long RC interconnect chain.
5. Current mode interconnects

In current mode signaling, information is represented as current signal. The theoretical model of current mode signaling is as shown in Fig. 3 [5].

The CMOS representation of current mode signaling is shown in Fig. 4. The receiver senses current signal at its input and provides low impedance.

Table 1 shows the delay analysis for both voltage and current mode interconnects [13-14]. It is analyzed that with proposed current mode interconnects delay decreases from 2.58 ns to 0.010 ns however power dissipation in the circuit increases from 22.01 µw to 19.33 µw. This is due to the low impedance at the receiver of current mode interconnect circuit. The delay analysis for current and voltage mode interconnect is shown in Fig. 10. It is seen that there is 79.84% reduction in current mode interconnect delay.

6. Conclusion

This paper presents second order transfer function designed with finite difference equation and Laplace transform at the source and load termination ends current mode signaling for delay estimation of current mode high speed VLSI interconnects. The perseverance of the current study is to estimate the delay of current-mode VLSI interconnects and to find the interaction between delay for various lengths, line inductances and load capacitances using existing voltage mode. All the benefits give current mode signaling an upper edge over the voltage mode signaling. At highly miniaturized technologies, interconnects with current mode signaling would be the best choice with the assistance of HSPICE tool.

References


