An Area Efficient Low Power FIR filter for ECG Noise Removal Application

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Abstract

This paper focuses on compact, low power VLSI implementation of fast FIR filter and its performance analysis using noise removal technique. FIR filter design is focused using fast FIR algorithm with symmetric coefficients rearrangement and modified carry save addition. A comparative area and power analysis is done using synthesis design tool. Static Timing Analysis (STA) is carried out to find the delay by adding the individual gate delays and net delays of each path. It also compares path delays against their required minimum hold time and maximum setup values. STA uses Simulation Program with Integrated Circuit Emphasis (SPICE) characterized data stored in the technology library to verify circuit’s timing. Synopsys Primetime is used for the timing analysis. The proposed fast FIR filter is used for the power efficient ECG noise removal technique that are widely popular in the field of biomedical and healthcare applications.

Key Words: Finite impulse response (FIR) filter, synopsys design tool, static timing analysis, ECG noise removal.
1. Introduction

VLSI technological advancement has created a major impact in most of the consumer applications and biomedical signal processing applications due to its high speed and low power. The low power consumption increases the life cycle of the VLSI based biomedical products (Rabaey 1996). The rapid technological scaling of the MOS devices leads to the integration of multiple applications on a single chip (Weste & Harris 2004). FPGAs are being increasingly used for a variety of computationally intensive applications, especially in the area of DSP (L. K. Ting et al, 2001). Due to rapid advancements in fabrication technology, the current generation of FPGAs contains a large number of configurable logic blocks (CLBs), used for a wide range of filtering applications. Most of the DSP design techniques currently in use are targeted towards hardware synthesis and do not specifically consider the features of the FPGA architecture (Dempster & Macleod 1995).

2. Implementation of Proposed FIR Filter

FIR filter is implemented using Equation (1), where \( p \) is the order of the filter, \( h_i \) are the filter coefficients, \( x(n) \) and \( y(n) \) are the \( n^{th} \) input and output signal samples, respectively.

\[
(y_n) = \sum_{i=1}^{p} (h_i x(n-i))
\] (1)

Muhammad et al (2001) developed the parallel transposed direct form architecture to work on real-time input data samples. Low-area multiplication process has been performed using the selection of radix-8 pre-multiplied coefficients and one-hot encoded bus. From the area and power consumption report, it was concluded that the developed design achieves compact layout design and reduced power dissipation.

In this paper, the computational complexity of FIR filter is successfully reduced using polyphase decomposition which is simple to implement. The idea of the polyphase decomposition is to divide the filter into number of subsystems by rearranging the filter coefficients. The polyphase decomposition provides the small size parallel FIR filters for complexity reduction and better performance, but the number of computations is not reduced. To improve the performance of the parallel FIR filter arrangement, fast FIR algorithms with symmetric coefficients rearrangement and modified carry save addition technique is used.

3. ECG Signal Processing

In ECG signal enhancement, the main aim is to separate the pure ECG signal from the undesired artifacts so that visual interpretation can be improved. Kim
et al (2010) discussed about the filter based ECG signal pre-processing. In this approach, the acquired ECG data are initially digitalized and sent to the signal pre-processing stage of filtering unit. The filtering unit reduces noises such as baseline wander, power line interference and high-frequency noise using two-stage finite-impulse response (FIR) filters. These filters are implemented using 10-tap structure. By adjusting the coefficients, FIR filters can be used as low-pass filter or as high-pass filter.

**Cardiac Arrhythmia**

Under normal circumstances, ECG waveforms have a predictable direction, duration, and amplitude. Owing to this nature, the various components of the ECG can be identified, assessed, and interpreted as normal or abnormal. Each heartbeat in the cardiac cycle of the ECG waveform describes the time evolution of the heart’s electrical activity, which is made of diverse electrical depolarization-repolarization outline of the heart. Any uncertainty of heart rate or rhythm, or variation in the morphological pattern, is an indication of an arrhythmia, which could be identified by the analysis of recorded ECG waveform (Gacek & Pedrycz 2011).

4. **Results and Discussion on Implementation of FIR Filter**

The proposed design is modeled using Verilog HDL and verified using test benches with a range of input combinations. The Hardware Description Language (HDL) code is synthesized using Synopsys Design Compiler targeting 65-nanometer Taiwan Semiconductor Manufacturing Company library and target technology (TSMC). Once the design is synthesized, the physical design flow steps are carried out to perform floor planning, placement and routing.

Physical design flow steps are:

1. Test circuits for the proposed architecture are carried out using DFT compiler from Synopsys.
2. Formal verification for the proposed model is carried out using Synopsys.
3. Timing analysis for the synthesized netlist is carried out using Prime Time.
4. Floor planning of the synthesized netlist is carried out using JupiterXT.
5. Placement and Routing of the synthesized netlist is carried out using Astro.

Physical verification of the netlist is carried out using Hercules and to generate GDSII, which can be sent for fabrication.
Table 1: Architecture and Power Comparison Report for Proposed 27-tap Filter

<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Dynamic Power (mW)</td>
<td>64</td>
<td>45</td>
</tr>
<tr>
<td>Cell Leakage Power (μW)</td>
<td>164</td>
<td>114</td>
</tr>
<tr>
<td>Number of critical paths</td>
<td>456</td>
<td>424</td>
</tr>
<tr>
<td>Number of ports</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Number of nets</td>
<td>180</td>
<td>180</td>
</tr>
<tr>
<td>Value of slack</td>
<td>0.29</td>
<td>0.17</td>
</tr>
</tbody>
</table>

The final chip of proposed FIR filter has 50 numbers of input output port, 180 numbers of net and 325364 numbers of logic cells. The dynamic power and leakage power are 45 mW and 114 μW respectively.

Final chip obtained using synopsis compiler that can be fabricated using either twin tub process or Silicon on Insulator (SoI) technology. The number of I/O ports, nets, cells and area are also visualized from the final chip. The level of power saving is higher than that of conventional approach.

Table 2: Area and Delay Comparison

<table>
<thead>
<tr>
<th>Length</th>
<th>Method</th>
<th>Total Area (Sq. μm)</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Fast FIR using symmetric convolution (Tsao &amp; Choi 2012)</td>
<td>27432</td>
<td>12.34</td>
</tr>
<tr>
<td></td>
<td>Proposed fast FIR using modified CSA</td>
<td>24124</td>
<td>9.10</td>
</tr>
<tr>
<td>72-tap</td>
<td>Standard fast FIR filter algorithm (Cheng &amp; Parhi 2004)</td>
<td>53443</td>
<td>21.52</td>
</tr>
<tr>
<td></td>
<td>Fast FIR using symmetric convolution (Tsao &amp; Choi 2012)</td>
<td>46120</td>
<td>18.54</td>
</tr>
<tr>
<td></td>
<td>Proposed fast FIR using modified CSA</td>
<td>44218</td>
<td>14.83</td>
</tr>
<tr>
<td>144-tap</td>
<td>Standard fast FIR filter algorithm (Cheng &amp; Parhi 2004)</td>
<td>81269</td>
<td>32.72</td>
</tr>
<tr>
<td></td>
<td>Fast FIR using symmetric convolution (Tsao &amp; Choi 2012)</td>
<td>74214</td>
<td>24.24</td>
</tr>
<tr>
<td></td>
<td>Proposed fast FIR using modified CSA</td>
<td>62927</td>
<td>18.21</td>
</tr>
</tbody>
</table>

From the Table 2, it is observed that for a 24-tap FIR filter, the proposed design occupies 24124 sq. μm area and the value of delay found is 9.1 ns which are comparatively lesser than that of existing FIR algorithms. The down arrow marks indicate the reduction in delay and hence improvement in speed of operation when the filter design changes from standard algorithm to proposed
algorithm. The area and delay increase with respect to the tap length, as the increased tap length requires more number of computational elements.

5. ECG Noise Removal Technique

In this method, the multiplier based conventional FIR architecture is converted into multiplier less architecture that can be applied for high frequency EMG noise removal from ECG signal. Low frequency components in Electrocardiogram (ECG) signal can be easily removed using digital filtering in automatic heart disorder diagnosis systems.

For designing of FIR low pass filter, windowing technique is used. In this technique, Kaiser, Rectangular, Hamming, Hanning and Blackman functions can be utilized with increased sampling frequency to reduce the spectral leakage.

Hannings window and Blackman window coefficients are calculated using Equations (2) and (3)

\[ w(n) = 0.5 \left(1 - \cos \left(\frac{2\pi n}{M-1}\right)\right), \quad 0 \leq n \leq M-1 \]  

(2)

\[ w(n) = 0.42 - 0.5\cos\left(\frac{2\pi n}{M-1}\right) + 0.08\cos\left(\frac{4\pi n}{M-1}\right) \]  

(3)

where \( M \) is window length

The coefficients of Blackman-Harris window are calculated by

\[ w(n) = a_0 - a_1\cos\left(\frac{2\pi n}{M-1}\right) + a_2\cos\left(\frac{4\pi n}{M-1}\right) - a_3\cos\left(\frac{6\pi n}{M-1}\right) \]  

(4)

where \( a_0 = 0.35875; \ a_1 = 0.48829; \ a_2 = 0.14128; \ a_3 = 0.01168 \)

![ECG Signal Processing System](image)

Fig. 1: ECG Signal Processing System

The proposed design is modeled using Verilog HDL and verified using test benches with a range of input combinations. The Hardware Description Language (HDL) code is synthesized using Synopsys Design Compiler targeting 65-nanometer Taiwan Semiconductor Manufacturing Company library and target technology (TSMC). Once the design is synthesized, the physical design flow steps are carried out to perform floor planning, placement and routing.
Steps for Proposed fast FIR filter based ECG Noise Removal

1. Collect the originally recorded ECG data from MIT-BIH database
2. Specify the ECG data to be denoised, sampling frequency, window function and tap length.
3. Apply the input signal into the filter and set the desired output.
4. Obtain the output of the filter and compare with the desired output.
5. Calculate the error signal and apply adaptive algorithm for the obtained signal.
6. Obtained signal is given to the proposed fast FIR filter with modified carry save adder. The filtering process is speeded up using fast FIR algorithm and partial products of multiplication process are combined using modified carry save adder.
7. Repeat step 5 and step 6 for the required number of iterations to get the denoised signal.
8. Save the denoised signal for clinical diagnosis.

Results and Discussion

ECG signal from MIT-BIH database is used for analysis of proposed FIR filter. The modified limb led ECG signal is added with Gaussian noise to obtain the corrupted ECG signal. The corrupted ECG signal is processed using proposed fast FIR filter based noise removal technique to obtain the noise free ECG signal as shown in fig.2

![Corrupted ECG and Denoised ECG](image)

Fig. 2: Denoised ECG Output Under 144 tap FIR Filter

6. ECG Noise Removal Technique

The proposed compact FIR filter is implemented using fast FIR algorithm with modified carry save addition to realize high performance and low power consumption. The performance of the proposed filter is analyzed through ECG noise removal technique. The result analysis shows that SNR(Signal to Noise Ratio) improves with reduction in the values of MSE(Mean Square Error) and...
MAE (Mean Absolute Error) when tap length and order of the filter are increased. The improvement in SNR value shows that filtering performance of FIR filter has enhanced due to narrow transition band which in turn due to raise in the order of proposed FIR filter.

References


