PIPELINED FAST FOURIER TRANSFORM FOR LOW POWER OFDM BASED APPLICATIONS

K. Vijayakanthan, M. Anand, M. Janakirani

1 Research Scholar, Dr. M. G. R Educational and Research Institute University, Chennai-95.
2, 3 Professor, Dr. M. G. R Educational and Research Institute University, Chennai-95.

Abstract: In this paper, an area-efficient low power fast Fourier transform (FFT) processor is intended for Multi Input Multi Output—Orthogonal Frequency Division Multiplexing (MIMO-OFDM) that consists of a modified architecture of radix-2 algorithm that is delineated as Radix-2 multipath delay commutation (R2MDC). Orthogonal frequency division multiplexing may be a widespread methodology for high data rate wireless transmission. OFDM is also united with multiple antennas at all the access point and mobile workstation to extend diversity gain and/or Enhance system capability on a time-varying multi path attenuation channel, leading to a multiple input multiple output OFDM system. This paper describes the planning of R2MDC FFT for implementation of MIMO OFDM transceiver exploitation FPGA targeted to future wireless local area network systems. The proposed system is pipeline radix 2 multipath delay commutation FFT has been designed for MIMO OFDM. The MIMO OFDM transceivers are designed consistent with the proposed OFDM parameters. A low-power economical and full pipeline design allows the time period operations of MIMO OFDM transceivers. The FPGA board has been developed to verify their circuit behavior and implementation of MIMO OFDM Transceivers.

Keywords: Radix-2 multipath delay commutation · Frequency division multiplexing · Multi input multi output—orthogonal frequency division multiplexing · Inverse fast Fourier Transform · Fast Fourier Transform · Discrete Fourier Transform

1. Introduction

Multiple input multiple output—Orthogonal frequency division multiplexing (MIMO-OFDM) has become a promising technique for future mobile transmission communication system due to its lustiness to frequency selective attenuation and its flexibility in handling multiple information rates [1, 2].

MIMO-OFDM is that the economical answer for transmitter and receiver antennas. Multiple antennas at either side of receiver and transmitter will improve the spectral potency and reliability in multipath weakening channels [3–5]. Consistent with [6], the cyclic prefix is assumed to be an extended than the channel delay unfold. The OFDM signal for every antenna is obtained by exploitation IFFT and may be detected by fast Fourier transform (FFT). Every OFDM block of constellation symbols is remodeled exploitation an inverse fast Fourier transform (IFFT) and transmitted by the antenna for its corresponding stream. The received signals at every antenna are equally broken into blocks and processed exploitation an FFT [7].
Bolcskei et al have bestowed an OFDM based mostly abstraction multiplexing theme, the information streams are 1st more experienced OFDM modulators and so launched from the individual antennas. Within the receiver, the individual signals are more experienced OFDM demodulators [8]. A strong improvement over standard OFDM was the introductions of multi-carrier code division multiplex (MC-CDM) OFDM by kaiser in [9].

In MC-CDM, instead of sending one symbol on every subcarrier as in standard OFDM, teams of symbols are multiplexed along by suggests that of orthogonal spreading codes and at the same time transmitted on a gaggle of subcarriers [10].

OFDM could be a multi-carrier system wherever information bits are encoded to multiple sub-carriers, in contrast to single carrier systems, all the frequencies are sent at the same time in time. OFDM offers many benefits over single carrier system prefer multipath impact immunity, easier channel equalization and relaxed temporal arrangement acquisition constraints. However it’s a lot prone to native frequency offset and radio front-end non-linearity. The frequencies utilized in OFDM system are orthogonal. Neighboring frequencies with overlapping spectrum will so be used. This property is shown within the Fig. 2, where A, B, C, D, and E orthogonal. This leads to economical usage of BW. The OFDM is so ready to give higher rate for identical Bandwidth [11].

3. Proposed Pipelined R2MDC

The radix-2 multipath delay commutation (R2MDC) is one among the reversed architectures of radix-2 FFT formula that is employed to reverse the values as quick as potential so as to method the values and to commutate the FFT inputs, the design shown within the Fig. one consists of various blocks that should be utilized in the R2MDC. Investigated Radix-2 pipelined streaming FFT block that is employed within the baseline MIMO-OFDM system [12]. However we have a tendency to use radix-2 multipath delay commutation within the proposed system.
One of the foremost simple approaches for pipelined implementation of radix-2 FFT algorithm is Radix-2 Multi-path Delay electrical switch (R2MDC) design. Figure four shows the radix-2 multipath delay commutation design with butterfly II structure. It's the best way to arrange information for the FFT/IFFT algorithm, the input knowledge file sequence square measure broken into 2 parallel data stream flowing forward, with correct distance between information components getting into the butterfly regular by proper delays. The 8-point FFT in R2MDC design is shown in Fig. 3. At every stage of this architecture half of the information flow is delayed via the Register and processed with the last half data stream.

The A input comes from the previous element twiddle issue multipliers (TFM). The B output is fed to future element, unremarkably BFII. In 1st cycles, multiplexors direct the computer file to the feedback registers till they're stuffed (position “0”). On next cycles, the multiplexors choose the output of the adders/sub tractors (position “1”), the butterfly computes a 2-point DFT with incoming information and therefore the information keep within the feedback registers. The multiplication by \(-j\) involves real-imaginary swapping and sign inversion. The real-imaginary swapping is handled by the multiplexors MUX in expeditiously and therefore the sign inversion is handled by change the adding-subtracting operations by mean of MUX. once there's a requirement for multiplication by \(-j\), all multiplexors switches to position “1”, the real-imaginary information are swapped and therefore the adding-subtracting operations ar switched.

The design of BFI and BFII supporting 2 receive chains is shown in Fig. 5a, b. In BFI structure the sample routing MUXs and DEMUXs at the input and output of the BF_RAMs are management led supported c2 and c3 control signals while the computation unit is management led by c1 control signal. The management signals are issued by the BFI controller. Depending on the programming of range of receive chains the additional BF_RAMs are enabled. WiMAX supports 1Rx and 2Rx, LTE supports 1Rx, 2Rx and 4Rx. supported the necessity further buffers may be extended to the present BF structure. The adders and subtractors in BFI and BFII are fully-pipelined and followed by divide-by-2 and misreckoning. The divide-by-2 is employed. The algorithmic program used here is to turn the radix-2 algorithmic program within the IFFT design and to interchange by R2MDC design so as to urge a low space than the present system.

4. FPGA Implementation of MIMO OFDM Transceiver

The applications like signal process and tele-communication need FFT implementations which may perform with less latency computations and little in size whereas exhibiting less power consumption. These process tasks are executed either by one, high frequency embedded processor or by exploitation an Application Specific integrated circuit (ASIC).
Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASIC) give completely different values to designers, and that they should be rigorously evaluated before choosing anyone over the opposite. FPGA has been recommended as an sanctioning technology [13-15] for the hardware platform as they provide the potential of hardware-like performance coupled with software-like programmability [14].

The register transfer Verilog internet list of the OFDM Transceiver, that is optimized for low power consumption and ASIC implementation, is employed as basic internet list for mapping on a Xilinx FPGA as shown in Fig six. The DCM installs a zero section delay between the inner and external clock and this permits employing a first in first out interface operational on the clock edges to transfer transmit information and received information. The FPGA implementation is optimized for power consumption by disabling the most internal clock once a purposeful unit isn’t operational. This derived clock is that the output of a buffered AND gate with the most internal units.

Table 1. Comparison results of proposed R2mdc IFFT architecture with existing radix-2 and radix-4 architecture

<table>
<thead>
<tr>
<th>Methods</th>
<th>Slices</th>
<th>Luts</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2MDC</td>
<td>186</td>
<td>146</td>
<td>1.065</td>
</tr>
<tr>
<td>FFT</td>
<td>308</td>
<td>412</td>
<td>2.125</td>
</tr>
<tr>
<td>Radix-2</td>
<td>280</td>
<td>140</td>
<td>2.252</td>
</tr>
<tr>
<td>FFT</td>
<td>308</td>
<td>412</td>
<td>2.125</td>
</tr>
<tr>
<td>Radix-4</td>
<td>280</td>
<td>140</td>
<td>2.252</td>
</tr>
</tbody>
</table>

This was the case within the equalizer wherever extra pipeline registers are another within the divider and within the information path of represented higher than, delay between every butterfly board presently permits base band transmission via ADCs and DACs as shown Fig. 6.

The FPGA board uses transmitter, receiver, and Viterbi decoder functions enforced within the Xilinx FPGA. We tend to another interpolator, decimator, random signal generator, and computer interface. The interpolator and decimator need 100-MHz clock frequency and also the alternative modules operate at the clock speed. This FPGA with computer interface is employed for displaying Bit Error Rate (BER) and Packet Error Rate (PER) results and dominant the transceiver, we tend to shall execute information transmission experiments in each base band and pass band channels.

The simulation results for R2MDC FFT algorithms are tested much by implementing within the Spartan 3E FPGA development board. The Quartus-II tool is employed to transfer the planning in to FPGA development board within the FPGA board, the reset signal input is connected to the right switch.

![Figure 9. RTL schematic of R2MDC FFT](image)

Figure 9. RTL schematic of R2MDC FFT

![Figure 10. Comparison results of proposed R2MDC with existing radix-2 and radix-4 architecture](image)

Figure 10. Comparison results of proposed R2MDC with existing radix-2 and radix-4 architecture

For the set binary inputs at the remaining switches, when the method within the FPGA, the outputs are seen in light-emitting diode displays within the board. These FPGA outputs also can be verified with simulation results obtained exploitation MODELSIM. The FPGA board has been developed to verify their circuit behavior and implementation of MIMO OFDM Transceivers.

The below simulation diagram is for R2MDC as shown in Fig. 7. The reset price is high and when it slow amount the worth is low whereas in reset is high the input value doesn’t taken into the method. The output value is occurred once the reset is low. FPGA Spartan 3E development board to illustrate the implementation of R2MDC FFT is as shown in Fig. 8. The register Transfer Logic schematic for R2MDC FFT that’s targeted to mapped on FPGA Spartan 3E is shown in Fig. 9.

5. Results
The prime objective is to construct a FFT so as to possess low power consumption and lesser space. The parameters power consumption and space occupancy got due consideration for comparison the planned FFT with different FFTs. We’ve designed all writing victimisation Hardware Description Language (HDL), to induce power, and space report, we tend to use Xilinx ISE design Suite 10.1 as synthesis tool and Model Sim 6.3c for simulation. The comparison of Radix-2 FFT and Radix-4 with planned R2MDC FFT is shown within the Table 1 and Fig. 10. The planned FFT offers higher result than Radix-2 FFT and Radix-4 FFT in terms of space and power consumption as shown within the Table 1 and Fig. 10.

6. Conclusion

We given a R2MDC pipeline FFT as MIMO OFDM system with a 100-MHz bandwidth, that is an area-efficient low power FFT processor for MIMO-OFDM transceivers implementation exploitation FPGA. The transceiver uses full-pipelined process and provides operations at minimum clock frequency. The performance of assorted FFT like Radix-2, Radix-4 and planned R2MDC were meted out and their performance were analyzed with relation to the amount of CLB slices, LUTs and Power consumption. We tend to demonstrated transceiver design appropriate for the advanced OFDM system. In this paper, we tend to conclude that the projected R2MDC design offers a lower space and fewer power than the present radix-2 and radix-4 rule design. The proposed design shows that it may be used for low power applications like MIMO-OFDM transceiver.

References
