MULTI-OBJECTIVE OPTIMIZATION METHODOLOGY FOR EFFICIENT CMOS OPERATIONAL AMPLIFIER IN THE DESIGN OF LOW POWER 2ND ORDER DT SIGMA DELTA MODULATOR

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Abstract

The aim of this work is to design an efficient operational amplifier for the DT sigma delta modulator. For a designer it is very time taking process to design an operational amplifier with the required specifications, so the present work will reduces the design time as well as increases the efficiency and accuracy. This work is categorized into two parts they are, getting optimal dimensions of the transistor by multi objective optimization algorithm in MATLAB and by using them operational amplifier was designed and utilized it in the proposed sigma delta modulator architecture using CADENCE Virtuoso Spectre circuit simulator. For designing the efficient operational amplifier, desired specifications like Gain (Av), Unity gain frequency (UGF), Phase Margin (PM), Power consumption (Pc) were given to the optimization algorithm and the resultant optimal dimensions were generated. Using these dimensions an op-amp is designed which is used in Sigma Delta modulator for achieving high performance measures of Signal-to-
calculated and observed the best results with lesser design time. Here the sigma delta modulator was simulated using 0.18µm CMOS technology with the power supply of ±700mV.

**AMS Subject Classification:** 65Y05, 65YO4, 65Y10.

**Keywords:** Operational amplifiers, two-stage op-amp, multi-objective optimization Algorithm, first order Sigma-Delta modulator and second order Sigma-Delta modulator.

1 Introduction

Microelectronics industry is distinguished by the raising level of integration and complexity. It aims at decreasing exponentially the minimum feature sizes used to design integrated circuits [1]. Nowadays, most analog sizing designs are done manually with some aid of simulation tools and equation-based models and the quality of the resulting circuit is dependent on the expertise of the design [2-3]. For a designer it is very challenging task to finish the design in time, so this work will try to reduce the designer time as well as to improve the efficiency of the design. An op-amp design consist of huge theoretical calculations which consumes more time and also as a human being can make some mistakes during theoretical calculations but an automated tool cannot so we look forward to design a MATLAB based tool to give optimal transistor dimensions of an op-amp for the desired specifications[4][5]. This was named as MOOA (multi-objective optimization Algorithm) which is designed by combining Multi Objective Genetic Algorithm with the necessary equations of individual topologies of Op-amp. To achieve the low power this design was carried with the supply voltage of ±700mV which is lesser than the half of the nominal voltage. The modulator is the analog part of sigma delta ADC, the resolution of the converter depends upon the order of the modulator. Generally order of the modulator is set by the sampling ratio.

![Block diagram of first-order sigma delta modulator](image)

**Figure 1:** Block diagram of first-order sigma delta modulator

It consists of an integrator and a comparator (ADC) in the
“delta modulation”. It is based on quantizing the change in signal by sample to sample rather than absolute value of signal at each level. Sigma or integrating is done at the input side of the converter of the output of DAC and the input signal. So this modulation is called as sigma delta modulation [4-5]. The feedback signal from the DAC is subtracted from the input signal by the summing amplifier, and then the error signal is filtered by the low pass filter integrator. The comparator works as at oversampling clock frequency and act as quantize or ADC. It compares the input signal against last sample signal to see if it is higher than the reference or not. The density of ‘1s’ and ‘0s’ forming a pulse stream at the output is the digital representation of the input analog signal.

This paper is organized in the following manner; Section II describes the design of Op-amp using MOOA. Section III Describe the sigma-delta modulator. Section IV Discusses the simulation results of proposed sigma delta modulator and comparison with other publications. Section V provides conclusion.

2 Design of op-amp using MOOA

In general mainly three op-amp topologies are used in the design of data convertors, so this section will concentrates the efficient design of basic three topologies using MOOA. For utilizing op-amp in sigma delta modulator or in any other ADC the designer mainly concentrates on these parameters they are Gain (Av), Unity gain frequency (UGF), Phase Margin (PM), Power consumption (Pc). So they are defined as input specifications to the Multi objective optimization Algorithm (MOOA) which gives the transistor optimal dimensions as a result. This algorithm was designed using equations for topologies of op-amp they are Two-stage CMOS Op-amp, folded cascode Op-amp and Telescopic Op-amp. The resultant optimal dimensions are used for further circuit simulations. This flow will be explained by using Figure 2.

Figure 2: Op-amp design flow using MOOA
low power op amp will reduces the power of modulator. For a high performance Sigma delta modulator it is necessary to have high gain and full swing for the op-amp to draw the next stages, unity gain frequency (UGF) for desired range of operation, high resolution and the order of the modulator will increases the accuracy; hence higher resolution implies lower quantization noise and as of increasing the order a better noise shaping will be observed, high over sampling ratio (OSR) will avoids the aliasing effect as well as increases the SNDR & SNR, Good phase margin is for better performance and stability, So the desired parameters for the op-amp to design a modulator is tabulated as Table 1,

Table 1: Comparison of op-amp topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>Gain</th>
<th>Output Swing</th>
<th>Speed</th>
<th>Power Consumption</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two-Stage</td>
<td>High</td>
<td>Highest</td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Telescopic</td>
<td>Medium</td>
<td>Medium</td>
<td>Highest</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Folded-Cascode</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
</tr>
</tbody>
</table>

Among all the above designs two stage op-amp was chosen as the best suitable for the design of second order discrete time sigma delta modulator.

Table 2: Desired input Specifications to MOOA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Gain</th>
<th>Phase Margin</th>
<th>UGF</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Value</td>
<td>&gt;80dB</td>
<td>60degrees</td>
<td>&gt;5MHz</td>
<td>&lt;50µWatt</td>
</tr>
</tbody>
</table>

GUI windows of designed MOOA for getting optimal dimensions of the two stage op-amp is given by

Figure 3: MATLAB simulation of two stage opamp
i.e. width and length of each transistor of two stage operational amplifier. The schematic is designed using these widths and lengths in cadence virtuoso 0.18µm CMOS technology which is shown below.

![Schematic of NMOS differential pair two stage CMOS opamp.](image)

Figure 4: Schematic of NMOS differential pair two stage CMOS opamp.

### 3 Sigma Delta Modulator

In general there are two types of sigma delta modulator architectures one is Continuous time sigma delta modulator and second one discrete time sigma delta modulator[6][7]. The basic difference between above to architectures is addition of switch circuit, in discrete time sigma delta modulator a switched capacitor op-amp will be used at the input level. This work deals with the discrete time 2nd order sigma delta modulator.

![Second order sigma delta modulator](image)

Figure 5: Second order sigma delta modulator

#### 3.1. Design of Sampling Circuit

The sampling circuit was designed by using the cell view of NMOS differential pair two stage CMOS op-amp and it is connected as,
A pulse signal (sampling signal) is applied at the gate input of the transistor and input signal is applied at the drain terminal of the transistor[8][9]. Since it is a NMOS transistor, when the pulse is in high state then transistor will be ON and signal will be transferred to source terminal. When the pulse is at low then the voltage value is hold[10].

3.2. Design of discrete time second order Sigma-Delta Modulator

The second order sigma delta modulator consists of two integrators, two mixers, a comparator and DAC at the feedback as shown in below. The proposed schematic diagram of a discrete time second order Sigma-Delta Modulator is given by

4 Result Analysis

Magnitude vs. frequency graph and phase vs. frequency plot for two stage op-amp is given by
From the magnitude and phase plot shown in Fig. 8 it can be seen that Gain is 86.8dB, Phase Margin and UGF are calculated at 0dB of Gain which are read as 65.2deg i.e. 180 - 124.8.5(from plot) = 65.2deg and 5.419MHz.

The simulation results are tabulated and compared with the other result in the table as,
Table 3: Comparison of Results

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Parameter</th>
<th>paper [3], (Year 2015)</th>
<th>Paper [4], (Year 2011)</th>
<th>Paper [6], (Year 2006)</th>
<th>Paper [8], (Year 2011)</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Technology (uM)</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>180n</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Power Supply(V)</td>
<td>±900 m</td>
<td>±900 m</td>
<td>±900m</td>
<td>±1.8</td>
<td>±700 m</td>
</tr>
<tr>
<td>3</td>
<td>Input signal (Hz)</td>
<td>500</td>
<td>10K</td>
<td>10K</td>
<td>20K</td>
<td>Up to 2.5K</td>
</tr>
<tr>
<td>4</td>
<td>Input clock (Hz)</td>
<td>250K</td>
<td>1.28 M</td>
<td>10 M</td>
<td>10.24 M</td>
<td>2.5K to 5M</td>
</tr>
<tr>
<td>5</td>
<td>Gain(dB)</td>
<td>52</td>
<td>48.5</td>
<td>-</td>
<td>-</td>
<td>86.8</td>
</tr>
<tr>
<td>6</td>
<td>Order</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>OSR</td>
<td>250</td>
<td>64</td>
<td>256</td>
<td>256</td>
<td>1024</td>
</tr>
<tr>
<td>8</td>
<td>SNR(_{\text{max}})(dB)</td>
<td>74</td>
<td>70.2</td>
<td>82</td>
<td>145</td>
<td>145, 39</td>
</tr>
<tr>
<td>9</td>
<td>SNDR(dB)</td>
<td>64</td>
<td>68.6</td>
<td>80.1</td>
<td>-</td>
<td>70</td>
</tr>
<tr>
<td>10</td>
<td>DR(dB)</td>
<td>-</td>
<td>-</td>
<td>83</td>
<td>-</td>
<td>139, 3</td>
</tr>
<tr>
<td>11</td>
<td>ENOB (Bits)</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>12</td>
<td>Power consumption (watts)</td>
<td>4.6µ</td>
<td>60µ</td>
<td>200µ</td>
<td>2.7m</td>
<td>35.6 µ</td>
</tr>
</tbody>
</table>

Conclusion

This paper presented a new methodology for designing low power Sigma Delta modulators using a combination of design automation and modern circuit design techniques. The developed modulator satisfies the initial design parameters assumed by the designer so this approach will reduce the designer time. This design is carried out with the 180nm CMOS technology at an operating voltage of ±700mV and the results are tested with the help of Cadence Virtuoso Spectre Circuit Simulator. Compared to previously reported modulators for such signal band width this work obtains one of best SNR, SNDR, ENOB and DR. For better noise shaping the second order was chosen.

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